LCLS II Phase Reference System

C. Xu*, Josef Frisch, Bo Hong, Steve Smith, Larry Ruckman
SLAC National Accelerator Laboratory, Menlo Park, CA 94025, USA
charliex@slac.stanford.edu

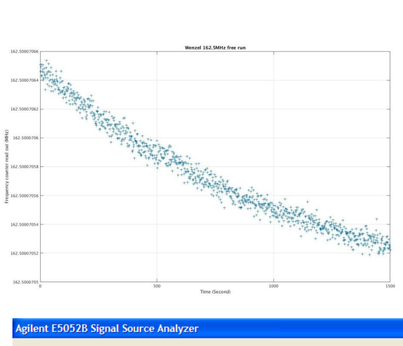
Abstract

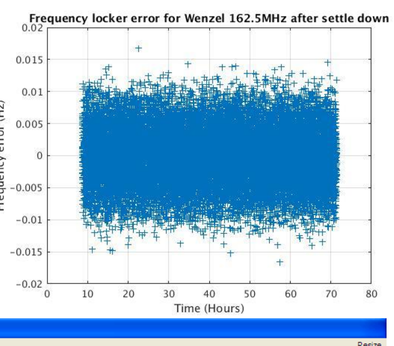
SLAC's LCLS-II is a next generation X-ray FEL that will use a CW 4 GeV superconducting. It will deliver both soft and hard x-ray FEL to users. When LCLS II turns on, it will produce X-ray laser that is 10,000 times brighter than LCLS I and produce X-ray pulses at one million times a second. In order to achieve this high level of performance, it is critical to have a stable RF reference system throughout the machine. We have designed a phase reference system that provides a reference signal for LCLS II at 1300MHz that has a measured integral jitter of 3.5fs from 100Hz to 10kHz. (Requirement is 10.7fs) They system also provides 185.7MHz reference signal for the Timing system, 1320MHz LO for the LLRF system, 476MHz synchronized reference for LCLS I, and other sub-systems. The 1300MHz reference features a bi-directional signal which allows the technic of phase averaging to eliminate phase drift caused by change in cable length. This poster will discuss the overall system design of the phase reference line system, which includes algorithm, hardware design, firmware design, and test result. It will also review the challenges we faced, as well as future improvements we wish to implement.

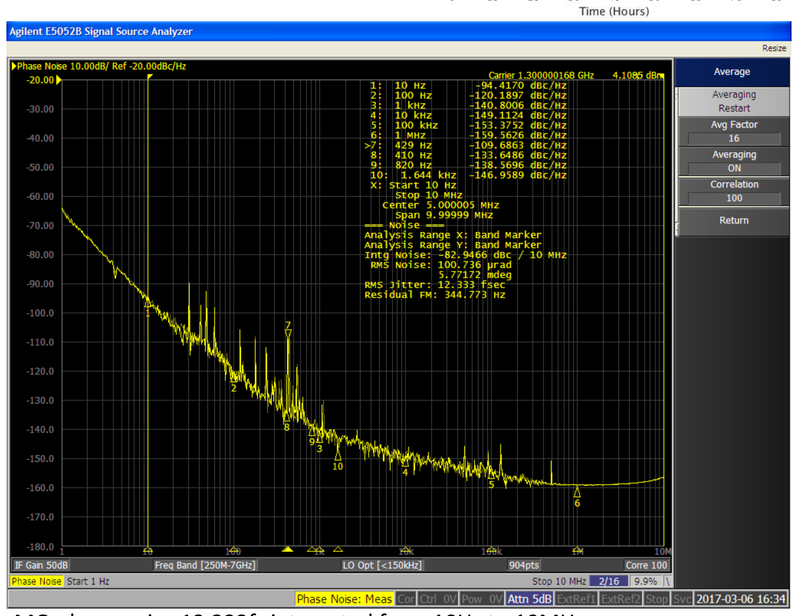
Requirements, Status, and Test Result

Timing Attribute	Value
Phase Reference (Linac RF)	1300 MHz
Clock (Gun RF = Linac RF/7)	185.71 MHz
Nominal Beam Rate (Clock/200)	0.92857 MHz
Fiducial Resync Freq (Clock/2600)	0.07143 MHz
Fiducial (Power Line Phase)	360 Hz
Stability – Phase reference line (PRL)	1 fs/sec, 1 ps/day
Jitter – PRL (100Hz to 10kHz)	0.005º or 10.7 fs

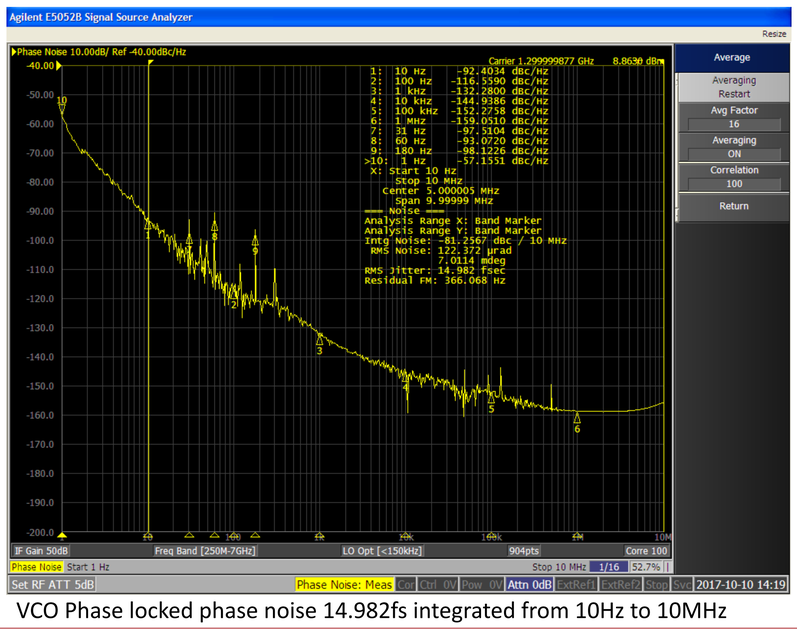
Currently the project is in the final assembly and testing stage. All the chassis has been fabricated. The laboratory test jitter result of the phase reference line achieves 3.5fs integrated from 100Hz to 10kHz, with the requirement set at 10.7fs. The frequency locker can keep the MO frequency locked at 162.5MHz within +/-0.01Hz on average with a 80Hr test in the laboratory.





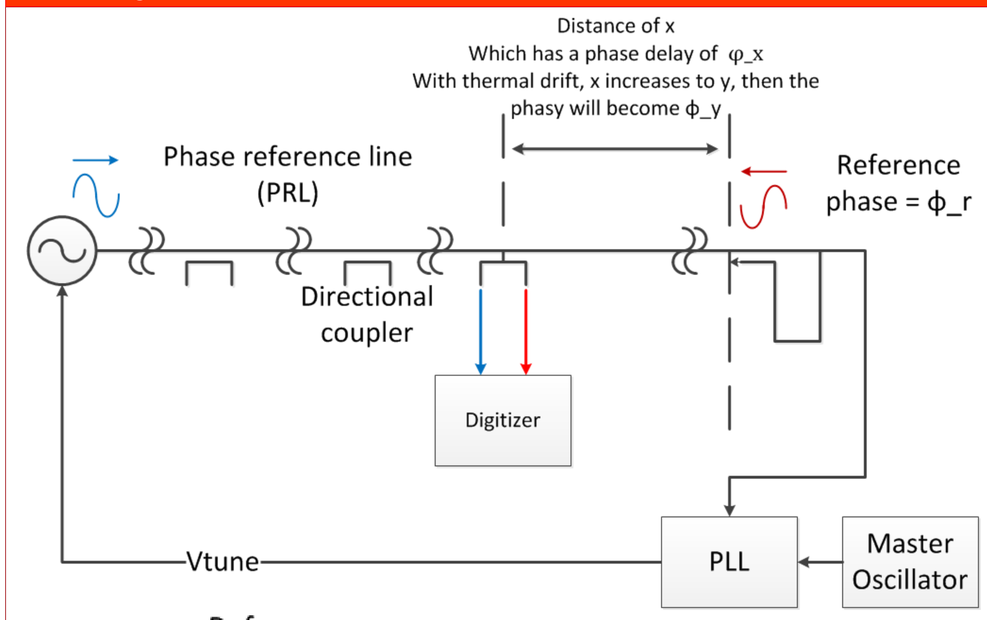


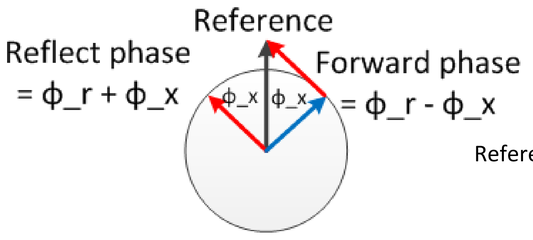
MO phase noise 12.333fs integrated from 10Hz to 10MHz



VCO Phase locked phase noise 14.982fs integrated from 10Hz to 10MHz

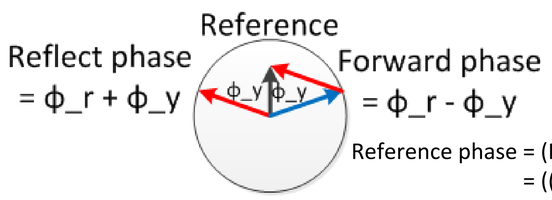
Phase Average





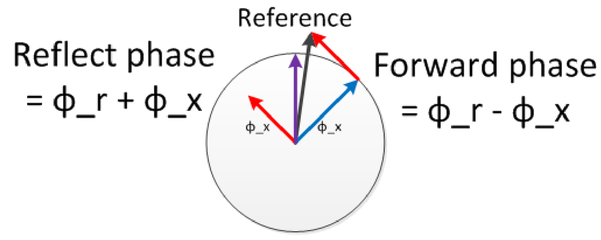
Reference phase = (Forward phase + Reflect phase)/2
= ((ϕ_r - ϕ_x) + (ϕ_r + ϕ_x))/2
= 2*ϕ_r/2
=ϕ_r

Temperature drift causing the phase reference line to expand. Which causes ϕ_x to expand by Δϕ, then the new phase delay caused by the PRL is ϕ_y = ϕ_x + Δϕ



Reference phase = (Forward phase + Reflect phase)/2
= (((ϕ_r + (ϕ_x + Δϕ)) + (ϕ_r – (ϕ_x + Δϕ)))/2
= 2*ϕ_r/2
=ϕ_r

In order to cancel out the thermal drift of the phase reference line, a reflectometer technique is used for the phase reference system. The VCO generates a "forward" signal from the opposite end of the master oscillator. When the VCO signal reach the master oscillator, the signal is reflected and enters the phase reference line again, thus creating the "reflection" signal. At any arbitrary point on the phase reference line, the directional coupler couples out the forward and reflect signal. Referencing to the master oscillator, the forward signal is ahead, and the reflection signal is lagging in phase. The amount of phase difference is determined by the length from the coupler to the master oscillator. Then the "forward" and "reflect" signal is digitized, and average of the two signal phase is calculated. This will give us the phase at the master oscillator. Because the phase of the "forward" signal is leading and the "reflection" signal's lag is both related to the distance from the coupler to the master oscillator, this will cancel out any thermal drifts from the cable.

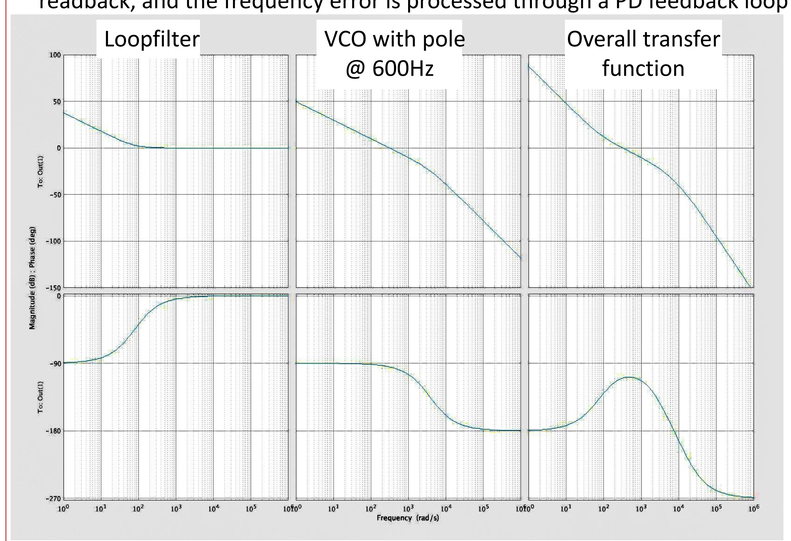


In this design, the phase averaging is performed inside a FPGA after the signal has been downmixed and digitized. If the averaging were to be done using analog components, then it would be very sensitive to amplitude imbalance. If forward and reflect signal's amplitude is not matched well, then there will be an error on the reference phase. If the amplitude were to change dramatically, then the reference will not be very accurate. By using the digital method, the reference phase will be more immune to amplitude imbalance and jitter. Although amplitude jittery will cause certain amplitude to phase conversion, the effect is not very significant.

Phase Locked Loop

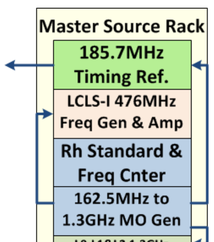
There are two PLL loops in the design. One VCO is at sector 0, and another at sector 4. The Master Oscillator (MO) is located in sector 4. Both VCOs are 162.5MHz, then multiplied up to 1300MHz. The phase error is compared at the MO, and the Vtune signal is transmitted as a digital value through a private VLAN fiber network back to a DAC module at sector 0 & 4. The DAC outputs an analog signal to complete the feedback. Comparing to sending an analog Vtune signal, this will prevent any noise pickup and losses through the cable.

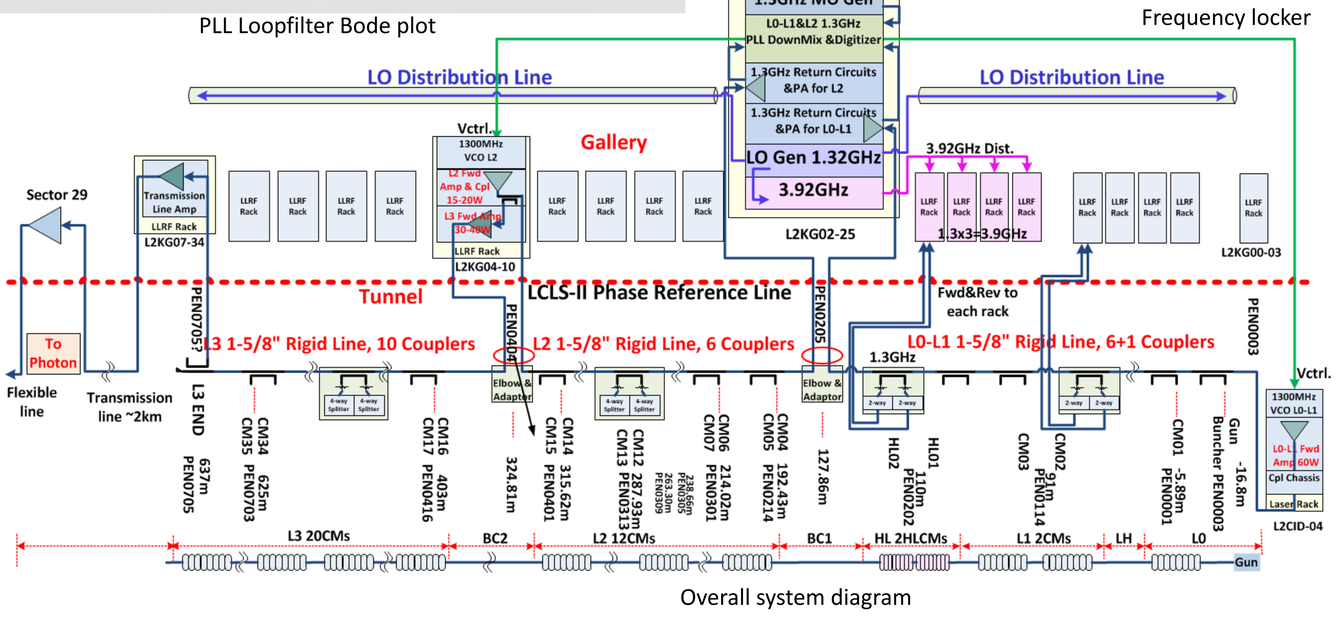
The 1300MHz MO and VCO is downmixed with The PLL algorithm is realized inside a Xilinx Kinex 7 FPGA. The loopfilter transfer function only has a zero and no pole. This is because the Wenzel VCO used has a pole around 600Hz. If there is another pole in the loopfilter, it will cause a peak in the phase noise measurement. In order to keep the MO at the right frequency, a frequency locker is implement using a frequency counter, and Rb standard as the frequency readback, and the frequency error is processed through a PD feedback loop in MATLAB.



PLL Loopfilter Bode plot

Frequency locker





Overall system diagram

U.S. DEPARTMENT OF ENERGY | Office of Science