Baseband Board Set for LCLS-II LLRF*

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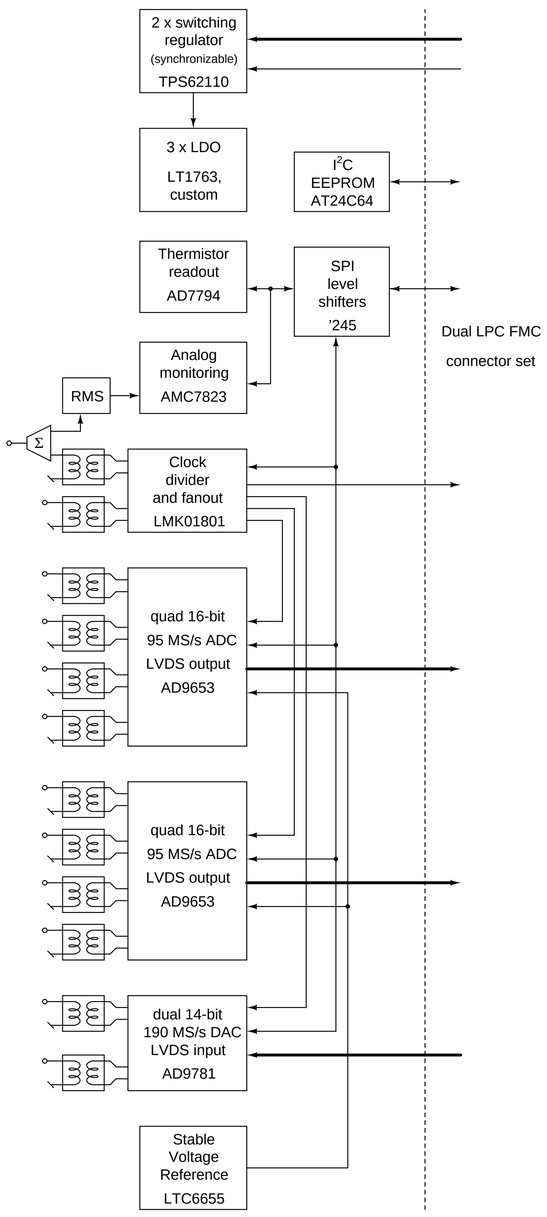
Abstract

The digitizer and FPGA hardware for any LLRF system together are the primary driver for determining system performance and capabilities. A two-board set has been developed, characterized, and applied by the LCLS-II LLRF four-lab collaboration. It is a high-performance, moderate-cost construction that could be adapted to related system designs. Eight 100 MS/s ADC inputs and two 200 MS/s DAC outputs give enough density to be useful controlling one or two cavities. The interconnect between the two boards electrically matches the dual FMC LPC standard, a plus for testing and upgradability. Eight application-side high-speed (12 Gb/s max) optical fiber pairs let this system participate in both local (rack-scale) and accelerator-wide communication networks. Robust housekeeping and board management features fit the needs of installation in an accelerator gallery, removing any fear of bricking the device during software updates. A single voltage supply and moderate power dissipation make it easy to build in to custom or semi-custom chassis. The board set was designed with analog performance in mind; careful testing using near-IQ sampling has revealed exceptionally clean RF noise spectra from 0.01 Hz to 1 MHz offset.

Initialization Trace

```
BMB7 Spartan-6 firmware information:
SHA256 bitfile hash:
82b054d3cb7c761e7f99dd25844c1ce3fbf5dcb5d2bcab726a6a86b06668d08a
Build timestamp:  1460677350 (2016-04-14 23:42:30)
Storage timestamp:  1464211181 (2016-05-25 21:19:41)
192.168.165.66
0x364c093 - Xilinx Kintex 7 160T
LBNL DIGITIZER V1.0 SN  017
Loading bitfile:  prc-20161126a.bit
Bitstream length:  6692572 bytes
Design name:  prc;UserID=0XFFFFFFFF;Version=2.16.1
Device name:  7k160tffg676
Build date:  20161126
Build time:  13:20:41
Length:  53540576 bits
Xilinx Kintex 7 interface selected
Bitfile lists git commit
9ec678cea84c0a187dd8e238bf1018fe5373c370
Attempting write of live json to .live_prc_regmap.json
AD9653 initialization
addr  U2  U3
000  18  18  SPI port configuration
001  b5  b5  Chip ID
002  61  61  Chip Grade
005  3f  3f  Device Index
008  00  00  Power Modes (global)
009  01  01  Clock (global)
00b  00  00  Clock divide (global)
00d  00  00  Test mode
010  00  00  Offset adjust (local)
014  02  02  Output mode
015  00  00  Output adjust
016  03  03  Output phase
018  04  04  V_REF
021  30  30  Serial output data control (global)
100  46  46  Sample rate override
109  00  00  Sync
AD9781 initialization
done
Polling SPI bus device reset -
amc write pg 1 saddr 0xc val 0xbb30
amc write pg 1 saddr 0xb val 0x8080
amc write pg 1 saddr 0xd val 0xffff
AMC7823 housekeeping voltages
 0   0.458 V    Spare (J14-9)
 1   1.135 V    V2P2V_MON (0.5 * V2P2V)
 2   1.866 V    V3P7V_MON (0.5 * V3P7V)
 3   0.991 V    V12P0V_MON (0.1776 * V12P0V)
 4   2.070 V    microphone
 5   1.047 V    LO_MON
 6   0.637 V    I_MON current * 1 Ohm
 7   1.643 V    V_MON (0.5 * VDD3P3V)
 8   0.111 V    On-chip temperature
test pattern 00001100
ADC clock 94.285 MHz
adc_value 1ac9 1ac9 8672 8672 8672 8672 8672 8672
test pattern 00001100
idelay  scan   U3DA  U3DB  U3DC  U3DD  U2DA  U2DB  U2DC  U2DD
idelay 00  Rx 1a c9 1a c9 86 72 86 72 86 72 86 72 86 72 86 72
idelay 01  Rx 1a c9 1a c9 86 72 86 72 86 72 86 72 86 72 86 72
idelay 02  Rx 1a c8 1a c9 86 72 86 72 86 72 86 72 86 72 86 72
idelay 03  Rx 09 c4 1a c4 86 72 86 72 c6 72 86 72 c6 72 c6 72
idelay 04  Rx 0d e4 1b e4 86 72 86 72 43 31 c6 31 43 72 43 31
idelay 05  Rx 0d e4 09 e4 86 72 86 72 43 39 42 39 43 72 43 39
idelay 06  Rx 0d e4 0d e4 86 72 86 72 43 39 43 39 43 72 43 39
idelay 07  Rx 0d e4 0d e4 86 72 86 72 43 39 43 39 43 31 43 39
idelay 08  Rx 0d e4 0d e4 86 72 86 72 43 39 43 39 43 39 43 39
idelay 09  Rx 0d e4 0d e4 86 72 86 72 43 39 43 39 43 39 43 39
idelay 10  Rx 0d e4 0d e4 46 72 86 30 43 39 43 39 43 39 43 39
idelay 11  Rx 0d e4 0d e4 42 71 46 70 43 39 43 39 43 39 43 39
idelay 12  Rx 0d e4 0d e4 43 39 42 39 43 39 43 39 43 39 43 39
idelay 13  Rx 0d e4 0d e4 43 39 43 39 43 39 43 39 43 39 43 39
idelay 14  Rx 0d e4 0d e4 43 39 43 39 43 39 43 39 43 39 43 39
idelay 15  Rx 0d e4 0d e4 43 39 43 39 43 39 43 39 43 39 43 39
idelay 16  Rx 0d e4 0d e4 43 39 43 39 43 39 43 39 43 39 43 39
idelay 17  Rx 0d e4 0d e4 43 39 43 39 43 39 43 39 43 39 43 39
idelay 18  Rx 0d e4 0d e4 43 39 43 39 43 39 43 39 43 39 43 39
idelay 19  Rx 0d f0 0d e4 43 39 43 39 43 39 43 39 63 39 43 39
idelay 20  Rx 8c 72 0d f0 43 39 43 39 a1 b9 43 bd a1 39 e3 b9
idelay 21  Rx 86 72 0c 72 43 39 43 39 a1 9d 63 9c a1 39 a1 9d
idelay 22  Rx 86 72 84 72 43 39 43 39 a1 9c a1 9c a1 39 a1 9c
idelay 23  Rx 86 72 86 72 43 39 43 39 a1 9c a1 9c a1 3d a1 9c
idelay 24  Rx 86 72 86 72 43 39 43 39 a1 9c a1 9c a1 9c a1 9c
idelay 25  Rx 86 72 86 72 43 39 43 39 a1 9c a1 9c a1 9c a1 9c
idelay 26  Rx 86 72 86 72 23 39 43 39 a1 9c a1 9c a1 9c a1 9c
idelay 27  Rx 86 72 86 72 21 39 43 1c a1 9c a1 9c a1 9c a1 9c
idelay 28  Rx 86 72 86 72 a1 3d 23 9c a1 9c a1 9c a1 9c a1 9c
idelay 29  Rx 86 72 86 72 a1 9c 21 9c a1 9c a1 9c a1 9c a1 9c
idelay 30  Rx 86 72 86 72 a1 9c a1 9c a1 9c a1 9c a1 9c a1 9c
idelay 31  Rx 0d e4 0d e4 43 39 43 39 43 39 43 39 43 39 43 39
idelay mirror 11 12 13 11 18 19 20 19 11 13 13 12 11 15 12 12
idelay mflags  2  2  2  2  2  2  2  2  2  2  2  2  2  2  2  2
test pattern 00001100
adc_value 0de4 0de4 4339 4339 4339 4339 4339 4339
adc_value 3493 3493 4339 4339 4339 4339 4339 4339
adc_value 4339 4339 4339 4339 4339 4339 4339 4339
BUFR 1 sync stopped after 2 iterations
BUFR 2 sync stopped after 0 iterations
bitslip:  test pattern 00001100
1111111111111111
0000000000000000
bitslip success after 1 iteration(s)
[0xa19c, 0xa19c, 0xa19c, 0xa19c, 0xa19c, 0xa19c, 0xa19c, 0xa19c]
Scanning adc_clk mmcm phase
 0     0     0     0     0     0     0     0     0
 5     0     0     0     0     0     0     0     0
10     0     0     0     0     0     0     0     0
15     0     0     0     0     0     0     0     0
20     0     0     0     0     0     0     0     0
Found safe mmcm phase 10
test pattern 00000000
AMC7823 housekeeping voltages
 0   0.458 V    Spare (J14-9)
 1   1.135 V    V2P2V_MON (0.5 * V2P2V)
 2   1.866 V    V3P7V_MON (0.5 * V3P7V)
 3   0.991 V    V12P0V_MON (0.1776 * V12P0V)
 4   2.071 V    microphone
 5   1.047 V    LO_MON
 6   0.622 V    I_MON current * 1 Ohm
 7   1.644 V    V_MON (0.5 * VDD3P3V)
 8   0.112 V    On-chip temperature
LBNL DIGITIZER V1.0 SN  017
```

Digitizer Architecture



Discussion

BMB-7

- XC7K160T application FPGA
- 8 × 12 Gbaud-capable fiber pairs (QSFP) for application
- 11 watt dissipation typ. + QSFP
- High-performance clock options support GTX
- Boots from network or on-board flash
- Always-on second FPGA (Spartan-6) manages power and booting using dedicated copper or fiber GigE
- Power supply and temperature monitoring

Digitizer

- 4 watt dissipation
- SMA: 8 × ADC, +6 dBm full-scale, tested at 20 MHz
- SMA: 2 × DAC, -5 dBm full-scale, tested at 145 MHz
- 2 x Pmod for chassis-level interfacing, e.g., interlocks and LEDs
- Clock input rated for 3.1 GHz (LMK01801)
- Separate clock-divider output provided at SMA
- Internal test points use U.FI
- Flat-back for thermal stabilization
- Serial number readout via human, QR code, or I²C
- BOM dominated by 2 × AD9653, board is manufactured for 2.4× that cost in qty. 25
- Automated board test process takes 5 min.

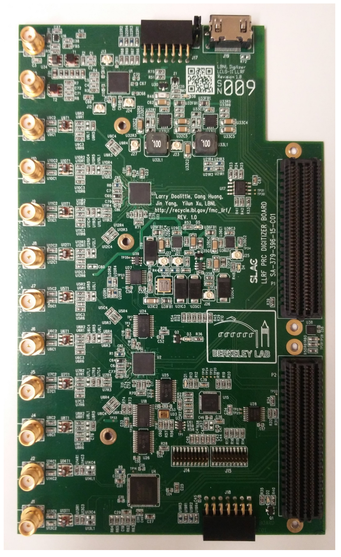
Power input is single-supply

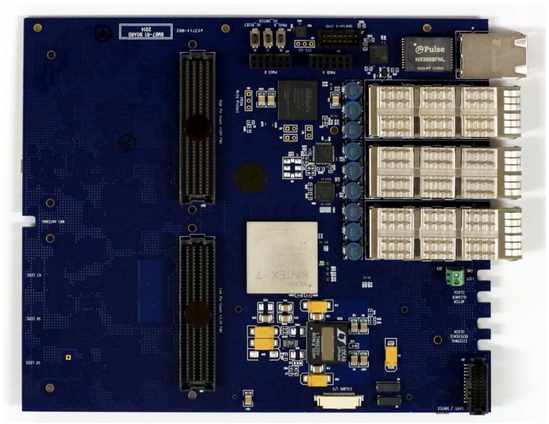
- nominally +12V but works from +6V to +15V

LVDS (not JESD204B) for high-speed digital

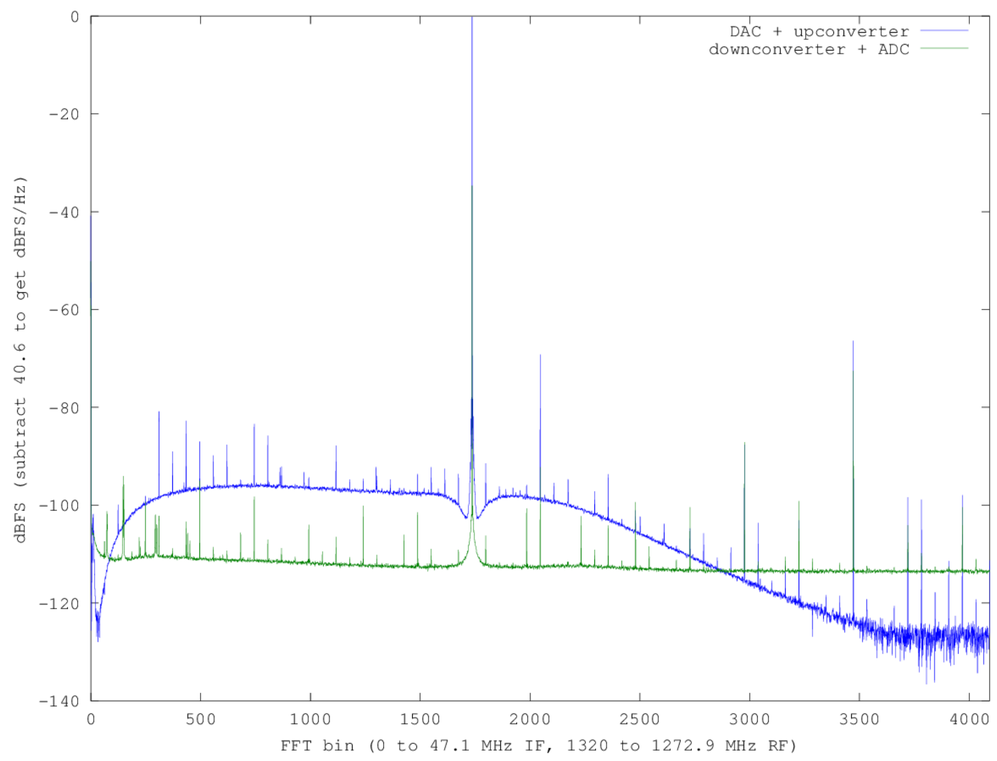
- 800 Mbaud LVDS lanes ADC ⇒ FPGA, 18 total
- 400 Mbaud LVDS lanes FPGA ⇒ DAC, 16 total
- AD9653 has really good *in-situ* test features
- FPGA fabric scans and auto-sets the FPGA idelay parameter all 16 ADC lanes handled in < 1 ms.
- Board support in Python, networks to BMB-7 over UDP

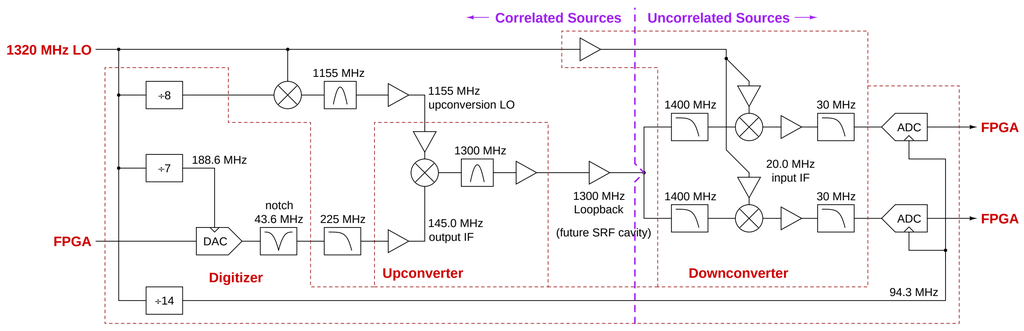
As-built photographs





Sample Test Results





Status

The LCLS-II LLRF system is entering its production phase. Pre-production boards have been manufactured and bench-tested as having excellent performance. Fifteen pre-production chassis have been assembled using this board set. Programming and testing on cold cryomodules is ongoing.

Office of Science
U.S. Department of Energy

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