The digitizer and FPGA hardware for any LLRF system together are the primary driver for determining system performance and capabilities. A two-board set has been developed, characterized, and applied by the LCLS-II LLRF four-lab collaboration. It is a high-performance, moderate-cost construction that could be adapted to related system designs. Eight 100 MS/s ADC inputs and two 200 MS/s DAC outputs give enough density to be useful controlling one or two cavities. The interconnect between the two boards electrically matches the dual FMC LPC standard, a plus for testing and upgradability. Eight application-side high-speed (12 Gb/s max) optical fiber pairs let this system participate in both local (rack-scale) and accelerator-wide communication networks. Robust housekeeping and board management features fit the needs of installation in an accelerator gallery, removing any fraying of the device during software updates. A single voltage supply and moderate power dissipation make it easy to build in to custom or semi-custom chassis. The board set was designed with analog performance in mind; careful testing using near-IQ sampling has revealed exceptionally clean RF noise spectra from 0.01 Hz to 1 MHz offset.

Abstract

The digitizer and FPGA hardware for any LLRF system together are the primary driver for determining system performance and capabilities. A two-board set has been developed, characterized, and applied by the LCLS-II LLRF four-lab collaboration. It is a high-performance, moderate-cost construction that could be adapted to related system designs. Eight 100 MS/s ADC inputs and two 200 MS/s DAC outputs give enough density to be useful controlling one or two cavities. The interconnect between the two boards electrically matches the dual FMC LPC standard, a plus for testing and upgradability. Eight application-side high-speed (12 Gb/s max) optical fiber pairs let this system participate in both local (rack-scale) and accelerator-wide communication networks. Robust housekeeping and board management features fit the needs of installation in an accelerator gallery, removing any fraying of the device during software updates. A single voltage supply and moderate power dissipation make it easy to build in to custom or semi-custom chassis. The board set was designed with analog performance in mind; careful testing using near-IQ sampling has revealed exceptionally clean RF noise spectra from 0.01 Hz to 1 MHz offset.

Introduction

The LCLS-II LLRF system is entering its production phase. Pre-production boards have been manufactured and bench-tested as having excellent performance. Fifteen pre-production chassis have been assembled using this board set. Programming and testing on cold cryomodules is ongoing.

Discussion

- XCT7610T application FPGA
- 8 x 12 Gb/s capable fiber pairs (QSFPP) for application
- 11 watt dissipation typ. = 0.25W
- High-performance clock options support GTX
- Boots from network or on-board flash
- Always-on second FPGA (Spartan-6) manages power and booting using dedicated copper or fiber GbE
- Power supply and temperature monitoring

Digitizer

- 4 watt dissipation
- SMA 8 x ADC, 6 dBm full-scale, tested at 20 MHz
- SMA 2 x DAC, 5 dBm full-scale, tested at 145 MHz
- 2 x Pmod for chassis-level interfacing, e.g., interlocks and LEDs
- Clock input rated for 3.1 GHz (LMK01801)
- Separate clock-divider output provided at SMA
- Internal test points use U.FL
- Flat-back for thermal stabilization
- Serial number readout via human, QR code, or I2C
- BOM dominated by 2 x AD9781, board is manufactured

As-built photographs

Status

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