

One-Turn Delay Feedback with a **Fractional Delay Filter**

Lorenz Schmid, Philippe Baudrenghien, Gregoire Hagmann CERN, Geneva, Switzerland

LLRF 2017 Barcelona

Overview Cavity Controller SPS TWC200

Biquad Filter with Fractional Delay Filter

- The Super Proton Synchrotron (SPS) at CERN accelerates protons and ions, which require a • large change in f_{rev} during acceleration. Acceleration performed by 200 MHz and 800 MHz travelling wave cavities.
- Travelling Wave Cavities (TWC) •
 - High bandwidth / low quality factor / low filling time (450 to 600 ns)
 - Different impedance seen by generator (RF) and beam (beam loading) [1] [2]:



- Beam loading is compensated with a **Biquad (IIR) filter**, *H*_{comb}
 - Homothetic repetition of peaks at $k \cdot f_{rev}$ in spectrum
 - $f_{\rm rev}$ is proportional to $f_{\rm RF}$, thus varies during acceleration
- Properties
 - Exact peak-to-peak distance of f_{rev} (around 43.3 kHz)
 - Low $\partial f_{rev}/\partial t$ change rate of maximal 492 Hz/s
 - High gain of 32 dB
 - Sampling frequency of 62.5 MHz
 - Bandwidth of ± 3 MHz around cavity center frequency, |A|*f*_{cav} (200.222 MHz) Extremely narrow resonance bandwidth of 100 Hz (single sided) Data path resolution of 24 bit signed

Filter Response



- LLRF feedback system compensates:

Update of existing TWC 200MHz cavity controller for the High Luminosity LHC upgrade (until 2020) [3] to achieve higher gain and therefore, allow compensation for higher luminosity:

Current System

- Sampling frequency and FPGA clock are coupled to f_{rev}
- Allows **fixed filter settings** for *H*_{comb}
- As f_{rev} is increased during one cycle (particle acceleration) so is f_{FPGA}
- **Varying** f_{FPGA} risks to create synchronisation issues



- Use fixed sampling frequency and FPGA clock, uncoupled to f_{rev}
- Adapt filter settings continuously to f_{rev}
- **Constant** f_{FPGA} , no synchroisation issues



- Peak-to-peak distance given by internal delay in Biquad filter Variable delay filter adapts internal delay to varying f_{rev} during \Rightarrow operation
- Variable integer delay:
 - Memory Element with variable integer delay via addressing
- Variable fractional delay:
 - Fractional Delay Filter (FDF) based on a 4th order Lagrange polynomial interpolation
- Low Pass Filter to avoid instabilities in closed loop feedback





Cavity Loop Simulation

VAmp Delay VAmp

Amplifie

Beam Generation

Cavity Model

- Complete low level RF simulation:
 - Cavity Controller
 - Cavity model (T. Mastoridis and J. Galindo)
 - Beam disturbance
 - Correct 1-Turn Delay
 - Up-/Down modulation around baseband
- Implemented in MATLAB Simulink / System Generator
 - Models based on S-functions
 - HW implementation for Xilinx Series 7
- Allows verifying cavity controller during f_{rev} variations









Simulation Frequency Response (Open Loop)







POSTER P-77

REFERENCES

[1] G. Dome, *The SPS Acceleration System*, Proc. 1976 Proton Linac Conf. Chalk River, Canada, 138-147 (1976) [2] P. Baudrenghien, G. Lambert, Reducing the Impedance of the Travelling Wave Cavities Feed-Forward and One Turn Delay

Feedback, Proc. of the Workshop on LEP-SPS Performance Chamonix, France, 94-101 (2000) [3] G. Hagmann & al., SPS LLRF Upgrade project, LLRF Workshop 2017, Barcelona, Spain, Poster P-92