# Spallation Neutron Source Low-Level RF FMC Module Development

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## Abstract

The original VME based Ring LLRF control system for the Spallation Neutron Source (SNS) was developed by project collaboration partner Brookhaven National Laboratory (BNL) and has been successfully operated for more than 10 years with beam power levels up to 1.4 MW. Insufficient spares, and hardware obsolescence, have led to the development of a new Micro Telecommunications Computing Architecture (µTCA) platform based system utilizing Commercial Off the Shelf (COTS) FPGA (Xilinx Kintex) carrier cards with dual FPGA Mezzanine Card (FMC) connectors and a Peripheral Component Interface Express (PCIe) interface to a Linux computer. Custom four-channel low latency 14-bit ADC / DAC RF data converter modules with external clock and trigger inputs were developed in house for the new Ring LLRF system. Following this design effort, multiple data converters and specialty function FMC modules have been developed to meet prototyping requirements for future Front-End, LINAC and Ring RF designs.

## Design Philosophy

All of the FMC modules are designed to be flexible and as simple as possible to meet our design needs. This began with our original dual DAC FMC design that evolved into the Dual ADC/Dual DAC FMC that we are currently utilizing in our µTCA based ring LLRF system. All of the designs follow the Vita 57.1 specifications so that the boards could be utilized on either a commercial or custom carrier card as long as the carrier supported the FMC Low Pin Count (LPC) connector standard.

## FMC 14-bit Data Converter Modules for 0.1 to 70 MHz RF Signals

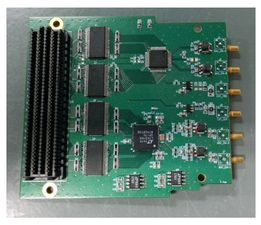
- Dual ADC Dual DAC
- Quad ADC
- Quad DAC

### Components

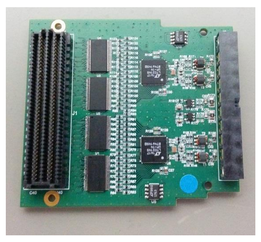
- DAC: Two channel 14-bit TI DAC5672A 275 MSPS
  - SNR 77 dB, SFDR 84 dBc, 4 clock cycles latency
- ADC: Two channel 14-bit Linear LTC2145 125 MSPS
  - SNR 73 dB, SFDR 90 dBFS, 6 clock cycles latency
- Connector: Vita 57.1 10mm LPC FMC

### Features

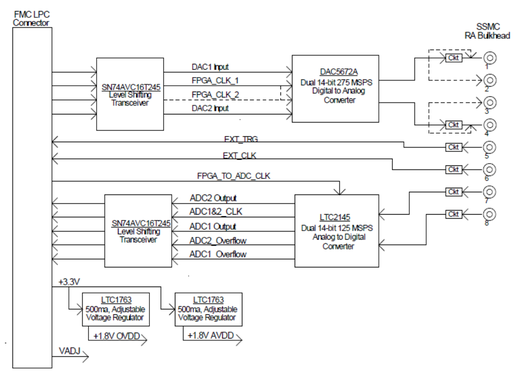
- 0.1 - 70 MHz AC coupled 50Ω ADC inputs and DAC outputs; DAC has option for DC coupling
- Two external clock/trigger inputs (AC or DC coupled)
- Designed to work with FMC VADJ at 1.8V, 2.5V or 3.3V
- Single ended parallel LVCMOS signaling using FMC LA IO pins
- FMC dimensions (69 x 76.5mm)



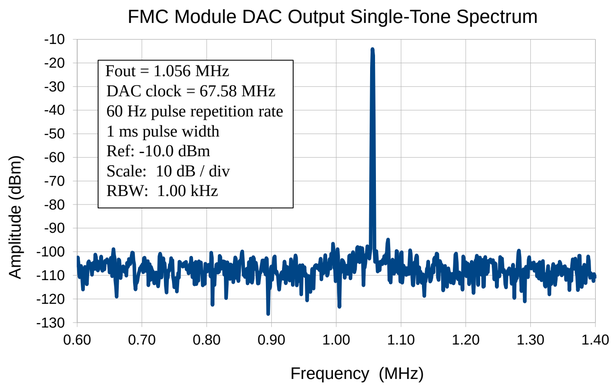
Dual ADC Dual DAC Module



Quad ADC Module




Dual ADC Dual DAC Module Block Diagram




DAC Single Tone Spectrum

## RF Coax Connector Evaluation

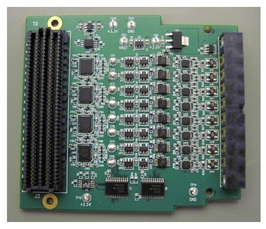
- Original SSMC connectors determined to be problematic
  - Cable connections difficult & connectors are delicate
- Replacement - Samtec GRF1 50Ω ganged RF connector
  - Investigated Molex Multi-Port RF (MPRF) solutions
- Initial testing has provided repeatable results
  - Phase measurement is repeatable on all connections
  - Insertion loss from the cable end through the board is -0.2 dB at 50 MHz and -1 dB at 805 MHz
  - VSWR is less than 1.3:1 on all connectors at 805 MHz
  - Channel to channel isolation is >70 dB on all connectors at 805 MHz
  - For the field control functions, all signals will be at 50 MHz

| Configuration | | | Return Loss | Insertion Loss | Crosstalk | |
|---|---|---|---|---|---|---|
| RF Drive | Measurement | RF Drive Frequency | S11 | S21 | Measured at J8 | Measured at J10 |
| Connector | Connector | (MHz) | VSWR | Log Mag (dB) | (dB) | |
| J2.2 | J9 | 1 | 1.03 : 1 | -0.06 | -85 | -83 |
| | | 50 | 1.09 : 1 | -0.19 | -95 | -96 |
| | | 805 | 1.27 : 1 | -1.02 | -74 | -72.8 |

RF Connector Evaluation

## 8 Channel RF Detector Module

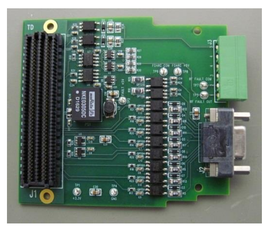
- Improves resolution and sampling speed for the High Power Protection Module (HPM)
  - 16-bit ADCs versus 10-bit
  - 5 MSPS versus 1.75 MSPS
- Improved RF detectors (AD ADL5513)
  - 1 MHz to 4 GHz bandwidth
  - 80 dB dynamic range
  - 20 ns response time
- Simplified calibration of channels
  - Planned automated calibration implemented
  - Use of digital potentiometers to set slope
  - $I^2C$ communication implemented and tested



8 CH RF Detector

## FOARC Detector Module

- Allows for the remaining High Power Protection (HPM) functions to be tested with the SNS carrier card
  - Provides the vacuum system interface to the HPM
  - Adequate arc detector inputs for a standard Super Conducting LINAC (SCL) system
  - Replicates the existing Machine Protection System (MPS) interface with improved isolation
- Required a miniature DB15 connector to fit the FMC requirements



FOARC Detector

## Single Link Timing Module

- Fully integrated into Ring LLRF µTCA system
- Outputs successfully tested to 68 MHz ($64f_{rev}$)

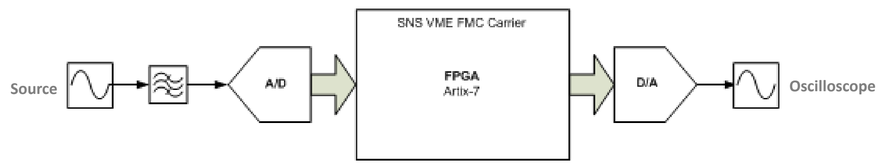
### Features

- (4) LVCMOS SSMC outputs → next revision: LEMO
- Decodes master timing system clock
- Recovers master timing reference clock

Timing Module

## FMC Data Converter Evaluation & Testing

- Successfully tested for use in the Ring LLRF µTCA system (1 or 2 MHz RF)
  - All components on board are specified to operate up to 70 MHz
- Simple loop-back testing completed, clocking ADC & DAC at 50 MHz
- Measured ~300 ns from output of source to input of oscilloscope
  - ~45 ns for filter and cables
  - ~120 ns for ADC (6 clock cycles)
  - ~80 ns for DAC (4 clock cycles)
  - ~20 ns for FPGA registers
- Preliminary spectral measurement shown in data converter section of poster.
- Noise performance measurements are still needed




## Lessons Learned

- Ganged RF connectors offer a more robust solution and shorten time required to install or change hardware
- The small Vita 57.1 standard module size presents challenges in component selection, functionality, and layout - this may be an issue in future designs

## Future Plans

The current suite of FMC modules has allowed us to quickly implement a replacement Ring LLRF system. The designs provide the building blocks necessary to support development work for the Linac LLRF replacement. The immediate plans are to finalize minor changes to the converter designs and release them for fabrication. The first replacement Ring LLRF system was installed in the accelerator in September and we will gain operational experience with the system in the next few months.

* This material is based upon work supported by the U.S. Department of Energy, Office of Science, Office of Basic Energy Sciences. This manuscript has been authored by UT-Battelle, LLC under Contract No. DE-AC05-00OR22725 with the U.S. Department of Energy. The United States Government retains and the publisher, by accepting the article for publication, acknowledges that the United States Government retains a non-exclusive, paid-up, irrevocable, world-wide license to publish or reproduce the published form of this manuscript, or allow others to do so, for United States Government purposes. The Department of Energy will provide public access to these results of federally sponsored research in accordance with the DOE Public Access Plan (http://energy.gov/downloads/doe-public-access-plan).
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