# Soc Architectures in LLRF at Fermilab Brian Chase, Joshua Einstein-Curtis, Matt Kufer, Kevin Martin, Philip Varghese - Fermilab, Batavia, IL

#### **SoC Architectural Benefits**

System-On-Chip (SoC) designs refers to devices where a front-end processing system is in the same package as peripherals, in particular an FPGA fabric. The tightly-coupled design allows for very high data rates, easily reaching several Gbps from an FPGA RF signal chain to front-end processing.

#### **General-Purpose LLRF System**



**Application diagram of SoCMFC Architecture** 

Fermilab has several teststands, for both superconducting and normal-conducting cavities and cryomodules. By using an SoC model, we have been able to minimize extra interfaces while providing an easy-to-manage testbed and control.

### µ2e, g-2 Controller Development

When upgrading the transfer lines for the new  $\mu^2e$  and  $g^{-2}$  experiments, it became necessary to integrate techniques used in the GP LLRF System and integrate with current VXI front-ends and systems. This involved More information can be found on P-11, 'LLRF System for the Fermilab Muon g-2 and Mu2e Projects'



**VXI-compatible controller Architecture** 

#### **Future Plans**

With more analog features being integrated on the same die as the application processor and FPGA, future designs will likely have a highlyintegrated analog conversion system. The rise of transceiver-based ADCs and DACs, in conjunction with the increasing density of high speed links in FPGAs, should lead to devices with a much smaller footprint than currently available.

(from HPS Handbook)

## **Marx Generator Control**

The Engineering Support group at Fermilab has begun using the SoC architecture for the new Marx Generators for the Linac klystrons. The SoC architecture allows for dynamic updates of the waveform based on pulse-to-pulse feedback. The system uses a CritcalLink Cyclone V MitySOM on a carrier board with Linear Tech ADCs and DACs



From Top left, clockwise - Marc Generator, Carrier Board with SOM, generated waveform



**Fermilab SoC-MFC Board Novtech NOVSOM CV** 



