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CONTRIBUTION TO THE ESS LLRF SYSTEM BY POLISH ELECTRONIC GROUP

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Abstract

Development of the LLRF system at ESS is coordinated by the Lund University, but part of it, LLRF systems for M-Beta and H-Beta sections, will be delivered within in-kind contribution from Poland. This document will describe the scope of work, work plan, and technical details of the selected components of the M-Beta and H-Beta LLRF systems sections.
Described contribution will be made by the Polish Electronic Group (PEG), a consortium of three scientific units. LLRF system for ESS will be made of both, commercially available components and components designed specially for this project, and those last ones will be presented and described here.

Polish Electronic Group

For the purpose of participation in ESS LLRF system development within polish in-kind contribution (IKC), a consortium of three polish research units has been established and called Polish Electronic Group (PEG). PEG consortium is made of National Centre for Nuclear Research (NCBJ) the consortium leader, Warsaw University of Technology (WUT) and Technical University of Lodz (TUL). All three institutions are experienced in development of the LLRF systems for FLASH and X-FEL. Due to common technologies, such as MTCA.4 [1], used in X-FEL and ESS, PEG members skills can be directly applied at ESS.

ESS LLRF SYSTEM AND SCOPE OF PEG CONTRIBUTION

LLRF System for ESS [2] will be implemented as FPGA based digital feedback system, based on the MTCA.4 electronics standard [1]. Planned M-Beta and H-Beta cavities will require 120 LLRF units in total, while in the period covered by the actual PEG IKC contract, only 80 LLRF units will be installed. Each LLRF unit will be single MTCA.4 crate, where both, commercially available and custom designed components will be used. PEG will design for ESS following devices:

- RTM Carrier Board low cost MTCA.4 board capable of supporting selected RTMs (Rear Transition Modules)
- LO generation and distribution unit
- Piezo driving and sensing unit for cavity resonance control
- Cavity Simulator for testing assembled LLRF systems and commisioning installed systems at ESS [3]

Except of mentioned custom designed components, PEG will be responsible also for assembling, testing, delivery and partial (in-rack) installation of the 80 LLRF systems for the M-Beta and H-Beta cavities.

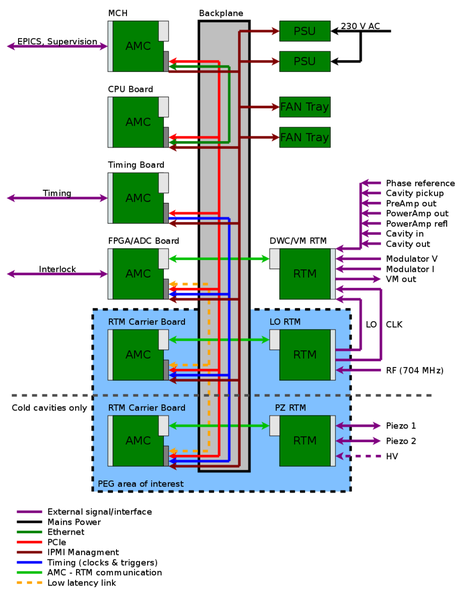

Figure 1: General layout of single ESS LLRF unit, custom designed devices has been marked with the rectangle at the bottom

RTM Carrier

RTM Carrier will be simple and low-cost FPGA based board, which will be focused on the providing minimal resources required to support LO generation RTM and Piezo Control RTM.
Main features:

- Artix-7 FPGA device (Latest family with gigabit transceivers, low cost)
- DDR3 memory (1 GB)
- Zone 3 (RTM) support, pin assignment compatible with DESY D1.0
- MMC (IPMI) support (mandatory LEDs, Hot-Swap handle, sensors, etc).
- PCI Express support on AMC ports 4-7 (x1, x2 or x4).
- MLVDS clock and trigger lines on AMC ports 17-20.
- Low latency links on AMC ports 12-15 (optional, if PCI Express is x1 or x2).
- USB-Serial for debugging
- Programmable clock manager, clock cross-switch and other clocking infrastructure

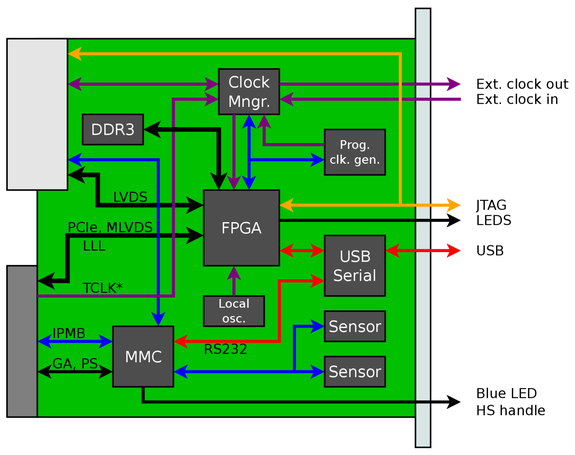

Figure 2: RTM Carrier block diagram

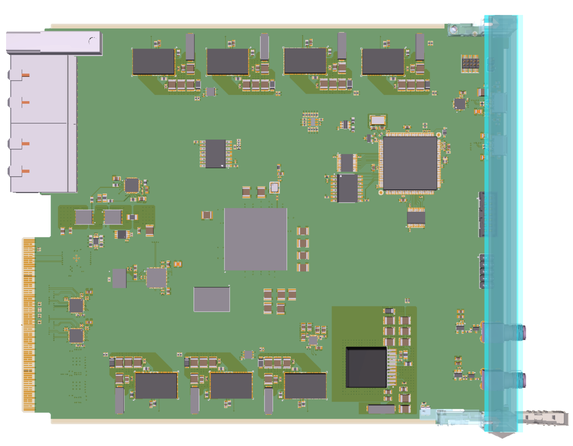

Figure 3: RTM Carrier 3D PCB model

LO Generation RTM

LO Generation RTM device will be responsible for generation of the local oscillator (LO) clock signal for down-converters. This device will be made in the MTCA.4 RTM form factor and will be supported by the RTM Carrier board. Single unit of the LO RTM will generate LO signals for 4 LLRF systems.

Main parameters and requirements:

- Reference input: 352.21 MHz or 704.42 MHz
- LO outputs frequency: 352.21 MHz + IF or 704.42 MHz + IF
- CLK frequency: 88,0525 MHz, 110,065625 MHz
- REF frequency: 352.21 MHz or 704.42 MHz
- LO signal output phase noise: Additive jitter of LO output signal integrated in the 10 Hz - 10 MHz band should be lower than 100 fs (704 MHz + IF) or 200 fs (352 MHz + IF).

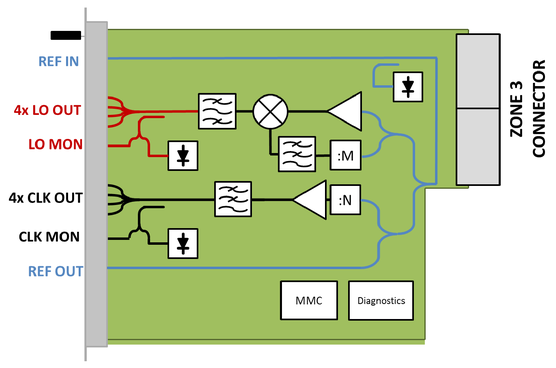

Figure 4: LO RTM block diagram

Piezo Control Unit

This device will be responsible for cavity resonance control, in addition of the LLRF cavity field control. It has been decided that piezo driver will be realized as a MTCA.4 RTM component. In order to mitigate the risk of driving high voltage (-/+ 100V) from MTCA crate, the solution with external power supply has been agreed.
At the actual stage, a prototype device has been created and successfully tested at Freia in spoke cavity test stand. The prototype is made of following components (from top to down):

- Piezo Driver module 1
- Piezo Driver module 2
- DC/DC Boost converter
- AMC carrier module with MMC

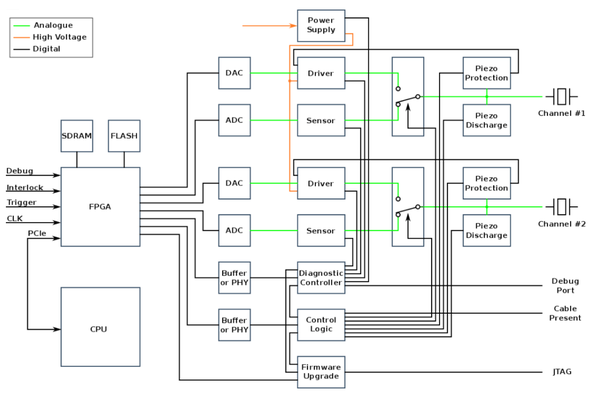

Figure 5: Conceptual block diagram of the piezo resonance control system

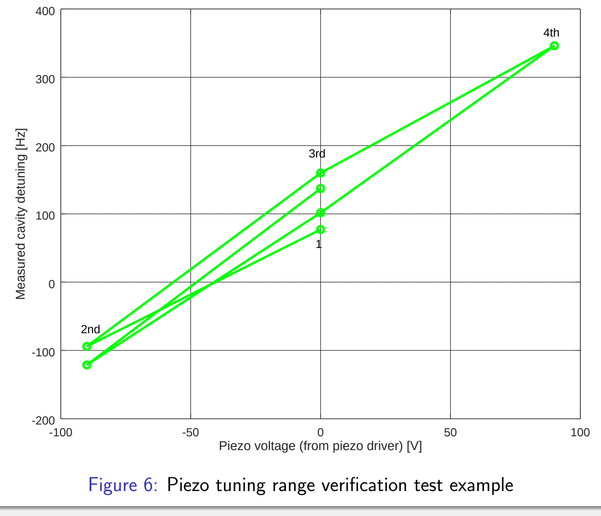

Figure 6: Piezo tuning range verification test example

Figure 7: Piezo control prototype device

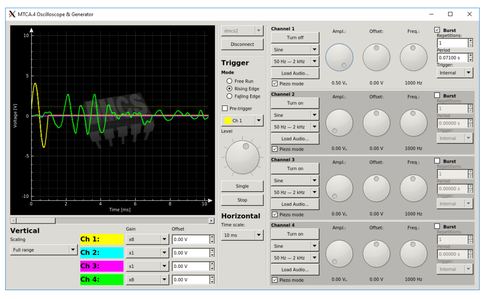

Figure 8: Software tools prepared for piezo signals generation and acquisition management

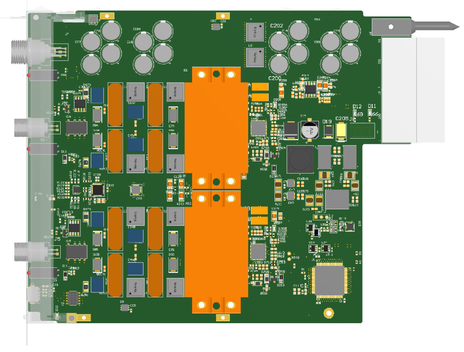

Figure 9: Piezo RTM device 3D model

References

1. MTCA, Micro Telecommunication Computing Architecture, https://www.picmg.org/openstandards/microtca/
2. A. J. Johansson and A. Svensson and F. Kristensen and R. Zeng, LLRF System for the ESS Proton Accelerator , in Proc. IPAC 14, Dresden, Germany, June 2014, paper WEPME079
3. M. Grzegrzółka, Cavity Simulator for the European Spallation Source, LLRF 2017 Workshop, Poster P-90

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