The Structure and Status of the LLRF System for PAL-XFEL

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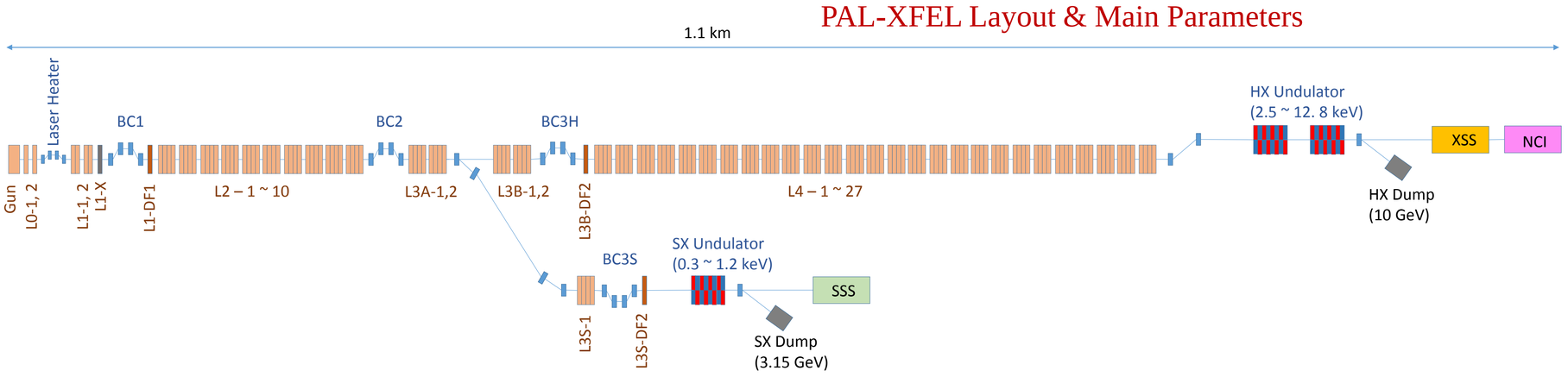
Abstract

PAL-XFEL was constructed as a hard X-ray free electron laser(FEL) following LCLS, and SACLA at the end of 2015. There are now many commissioning or ongoing projects like Euro-XFEL, SwissFEL and LCLS2 to mention a few. PAL-XFEL linac is mainly composed of S-band normal-conducting travelling-wave accelerating cavities and accelerates electron bunches up to 10 GeV. The commissioning and user service of the machine were realized sequentially and successfully without any critical issues since its construction. The LLRF system of PAL-XFEL has been operated stably for over 1.5 years since its initial operation in 2015. The LLRF system is composed of PC based platform, digital back-end, and analog front-ends. The analog parts include local signal and clock generator, upconverting transmitter, and downconverting receiver. At PAL-XFEL including this LLRF system, we achieved the electron energy jitter about 0.02 % (rms), the photon arrival time jitter about 20 fs (rms), and 0.1 nm SASE lasing.

PAL-XFEL Layout & Main Parameters



Parameter	Design (Hard/Soft)	Hard	Soft	Unit
Charge / bunch	0.2	0.14	0.14	nC
Slice emittance	0.5	0.55	0.55	mm·mrad
Electron energy	10/3.15	9.47	3.0	GeV
Pulse repetition	60	30	30	Hz
e^- peak current	3.0/2.5	2.5	2.2	kA
FEL gain length	3.6/1.8	3.61	2.08	m
FEL λ	0.1/1.0	0.104	1.52	nm
Photons / pulse	2.6/10	1.8	10.0	10^{11}

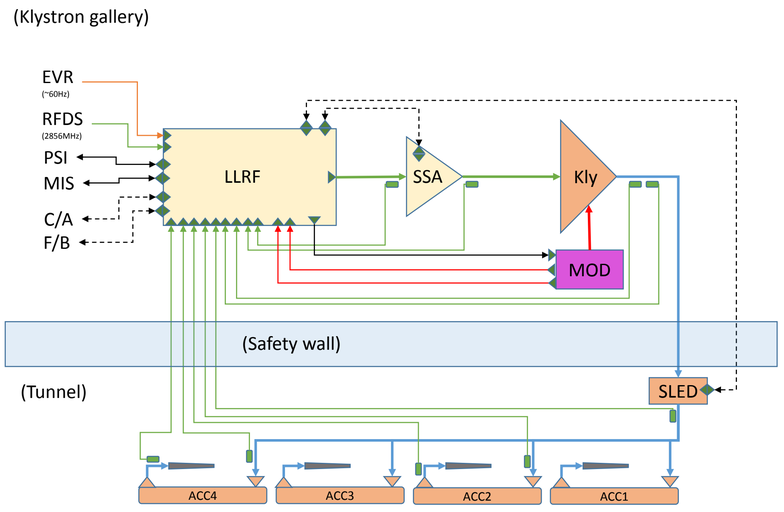
* Table based on Ref. : H.-S. Kang et al, First demonstration of consistent 20 femto-second timing stability of a hard X- ray free electron laser, Nature Photonics (Accepted)

RF System Configuration

- Normal-conducting TW cavities (except gun : SW 1.5 cell cavity)
- f_0 = 2.856 GHz (accelerating, deflecting), 11.424GHz (linearizer, 1 cavity)
- Total 51 RF stations
- Injector, linearizer, deflectors: 1 cavity for each klystron, modulator, SSA and LLRF
- L1 : 2 cavities for each klystron, modulator, SSA and LLRF
- L2, L3, L4 : 4 cavities for each SLED, klystron, modulator, SSA, and LLRF
- Hard X-ray (HX) : 49 stations for 10 GeV e^-
- Soft X-ray (SX) : 21 stations for SX (19 shared with HX) for 3 GeV e^-
- RF pulses ≤ 4 μs , Repetition rate ≤ 60 Hz
- Types of klystrons: S-band 80MW, 25 MW from Toshiba & X-band from SLAC

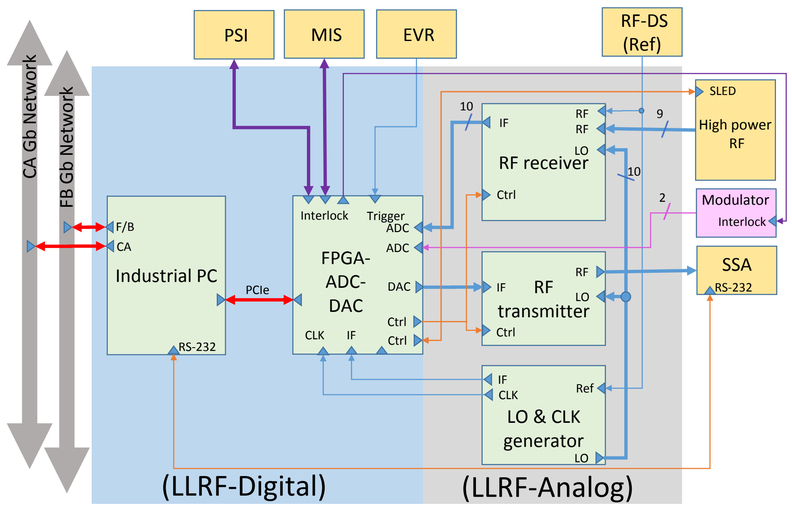
RF Station

- Example of the most occupying RF station
- The RF pulses generated within LLRF into RF power chain
- RF pulse detection from the various points (9 points)
- Klystron-beam-voltage and -current detection
- Fast interlock between pulses
- Dual Ethernet communication

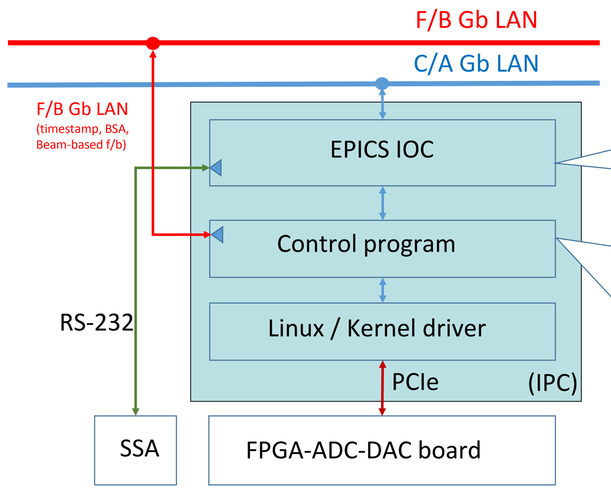


LLRF structure

- 3 modular parts : Analog frontends, FPGA-ADC & DAC, Processing PC
- Analog frontends : LO & CLK generator, Transmitter(Tx), Receiver(Rx) modules
- Freq. : Ref.=2.856 GHz, RF=2.856 GHz(11.424 for X), IF=29.75 MHz, CLK=119 MHz
- LO & CLK gen. : generation using frequency division and mixing
- Rx : 10 channels, IQ demodulator IC, standard IQ-sampling, reference tracking
- Rx sensitivity : <0.008 %, <0.008 ° in pulse-to-pulse RMS amplitude and RMS phase
- Tx : IQ modulator IC, IF IQ wave, high-speed switch for PSK and ON/OFF
- FPGA-ADC & DAC : PCB board specially developed for PAL-XFEL (12 16-bit ADCs & 2 16-bit DACs, Virtex-6 FPGA)
- Process PC : i5 CPU, 8GB RAM, 256GB SSD, PCIe, dual Gb LAN



LLRF Data-processing Structure



- PV update up to 120 Hz
- Control & setting PVs : user → control program
- Monitor PVs : control program → user

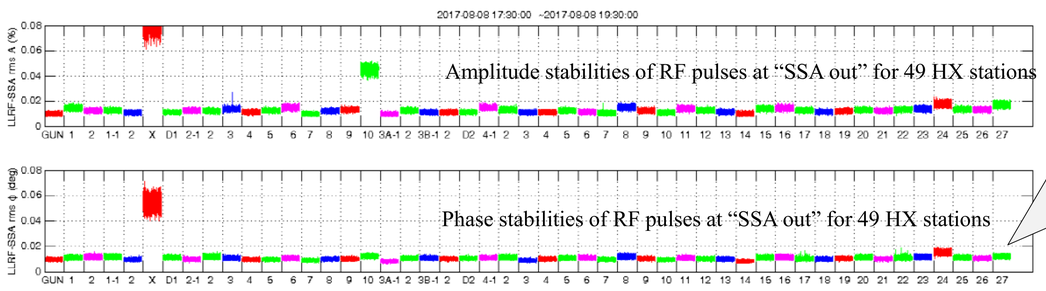
- Real-time(RT) data processing (A, ϕ, RMS,…) up to 120 Hz
- Real-time pulse-to-pulse feedback up to 120 Hz
- Real-time data saving & transmission for BSA & FDS
- Raw waveform processing (A, ϕ,…) at 2 Hz
- Receive timestamp via F/B LAN
- Receive beam-based feedback target via F/B LAN
- RT Interlock processing based on RT, non-RT data (HW interlock within FPGA)

SSA

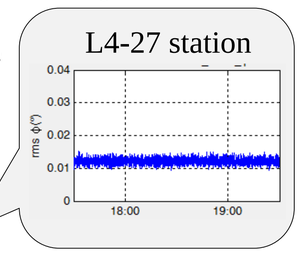
- Multi-stage amplification using solid-state technology
- S-band SSA based on LDMOS transistors
- X-band SSA based on GaN transistors
- Generation up to ≤900 W (S) & ≤1600 W (X) pulses

Performance

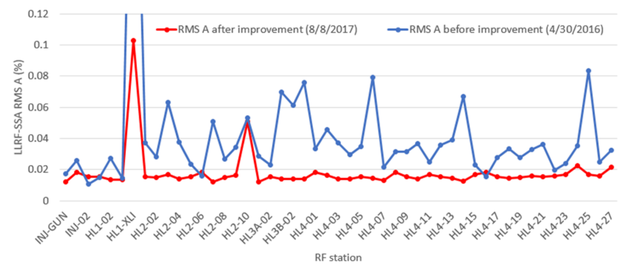
Collective plot of LLRF-SSA stabilities measured by LLRFs for 2 hours

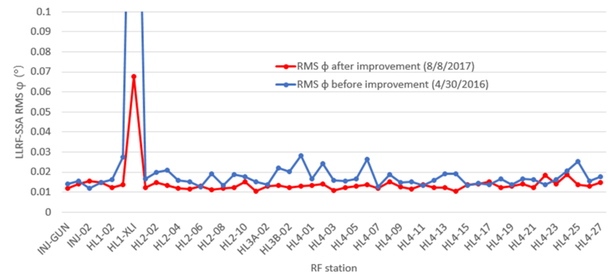


Magnified view:



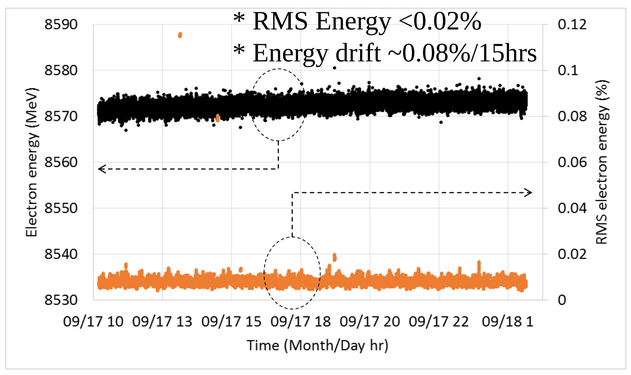
Comparative plot of LLRF-SSA stabilities between recent & past → A 130%, φ 60% improved !





Electron energy at linac-end provided recently

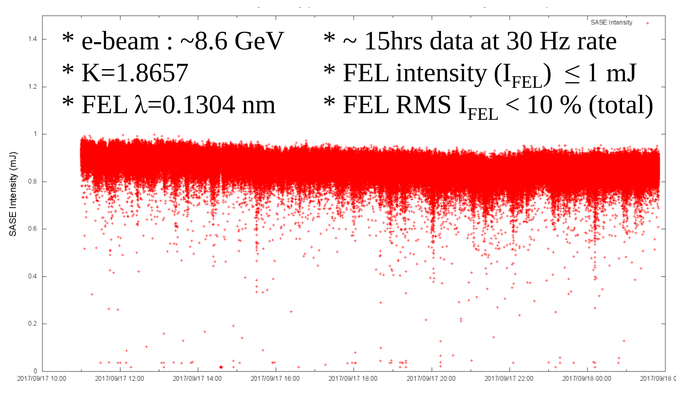
* e-beam : ~8.6 GeV
* RMS Energy <0.02%
* Energy drift ~0.08%/15hrs



* RMS calculation using 30 samples at 1 Sa/sec.

Recent X-Ray provided for user experiment

* e-beam : ~8.6 GeV
* K=1.8657
* FEL λ=0.1304 nm
* ~ 15hrs data at 30 Hz rate
* FEL intensity (I_{FEL}) ≤ 1 mJ
* FEL RMS I_{FEL} < 10 % (total)



* RMS calculation using total data for 15 hours.

Conclusion & outlook

- The PAL-XFEL machine began user service in 2017 after commissioning for over 1 year.
- LLRFs and SSAs have been in reliable and stable operation supporting PAL-XFEL for over 1.5 years.
- LLRF system is presented at the aspects of hardware and software structures and the performance.
- The PAL-XFEL recently generated electron energy 8.6 GeV at 30 Hz pulse-repetition rate showing energy jitter less than 0.02%, and excited X-ray of nearly 1 mJ and 0.13 nm with lasing jitter less than 10 %, which was supplied to user experiment.
- The efforts to improve the RF stabilities at accelerating cavities will be continued with some clues.