LLRF Upgrade Plans for PSI's Proton Accelerator

PAUL SCHERRER INSTITUT

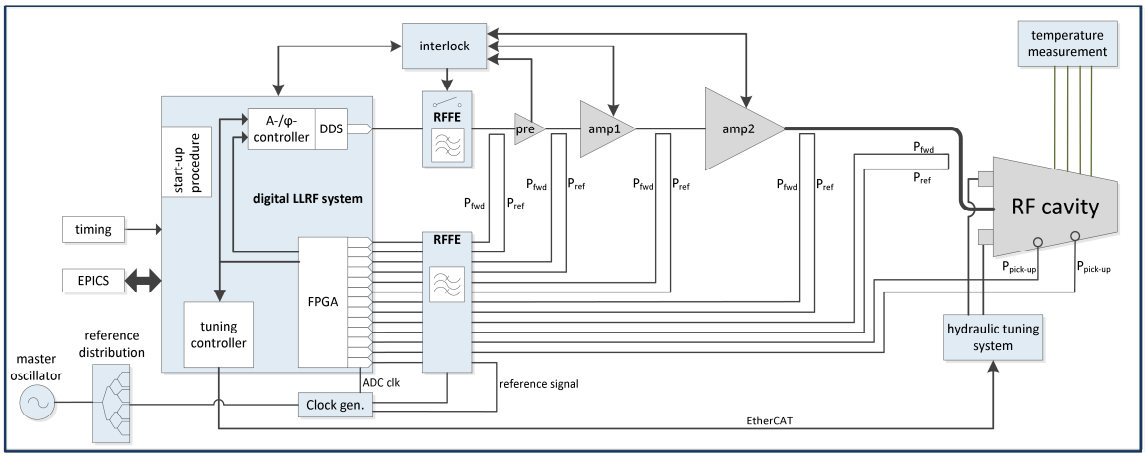
LLRF

Andreas Hauff, Roger Kalt, Stefan Mair, Patrick Pollet, Thomas Schilcher, Markus Schneider

Abstract

The high-intensity proton accelerator (HIPA) at PSI is a cascade of three accelerators that delivers a proton beam of 590 MeV energy at a current of up to 2.4 mA. The main cavities of the Injector 2 and Ring cyclotron are operated in CW at a frequency of 50 MHz. The original, up to 30 years old analog low-level RF system has to be replaced by a state-of-the-art digital system. It improves the operability and maintainability due to better diagnostics capabilities and integration into the control system (EPICS). The concept foresees a new LLRF system that is based on PSI's standard processing board, FMC mezzanine cards and a specific RF front-end to condition the RF signal for direct sampling. The demodulated signals are used for amplitude and phase feedback, for monitoring and calculation of the drive signal for the mechanical cavity tuners. The whole RF station is protected by an interlock system that was originally designed for the SwissFEL accelerator. The commissioning of the first upgraded RF station is scheduled for the second quarter of 2019.

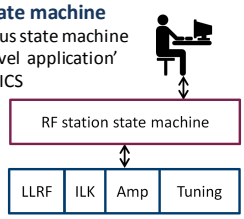
Overview of RF-Station for HIPA



Prove of concept	Exchange of Resonator 2	Exchange of Resonator 4 / Res. 2 operational	Resonator 4 operational
2017	2018	2019	2020 +

RF station state machine

- Asynchronous state machine as a 'high level application'
- Based on EPICS



HIPA Machine Parameters

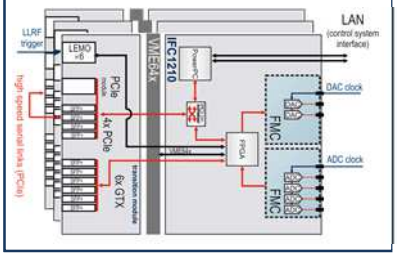
Beam energy	590 MeV
Beam current	2.4 mA
Main cavities	50.6 MHz CW
Reference frequency	50.6 MHz CW
Flattop cavity	151.9 MHz

Requirements for LLRF

Amplitude stability at 50 MHz	3e-4 rel.
Phase stability at 50 MHz	0.06°
Number of channels per RF station	16 or 24
Tube amplifier bandwidth	2 MHz
Tuning feedback bandwidth	25 kHz
A-/φ- feedback bandwidth	250 kHz

Carrier Card IFC1210

- Scalable system (PCIe, VME64x)
- The carrier board from IOxOS was already used in SwissFEL. It is based on a dual core processor from Freescale (P2020, 1.2 GHz). OS: Linux
- A FPGA Virtex-6 LX130T is used for fast data processing
- Firmware Event Receiver in FPGA (Timing) for synchronization of boards
- Rear transition card with I/O for e.g. interlock connection and fast optical links with SFP+-modules



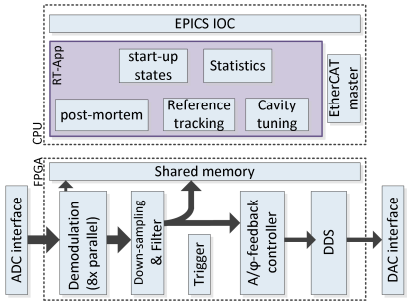
ADC/DAC

- Piggyback cards: FMC standard with HPC
- 8 Channel 16 Bit / 250 Msps
- DAC with 16 bit resolution operated at 253.2 Msps with pseudo-differential outputs
- FMC-cards use the switched power supply in the VME crate

Master Oscillator & Distribution

- The reference for the whole facility is a fixed-frequency master oscillator running at 50.63282 MHz. The reference is distributed with coaxial cables and power splitters with integrated amplifiers.
- The existing reference distribution is not drift compensated

Signal Processing



RF front-end in 19" box

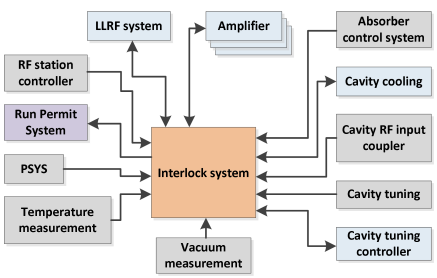
- Redundant PIN switches for interlock capability
- IF bandwidth is 30 MHz
- IF frequency is 50.6 MHz
- Channel to channel isolation is 80 dB
- Analog anti-aliasing filter
- Transparent RF level adjustment

LO & Clock Generation

- ADC clock frequency is a multiple of the reference frequency: $5 \times f_{ref} = 253.2$ MHz
- Optional LO generation for RF stations with 500 MHz cavities

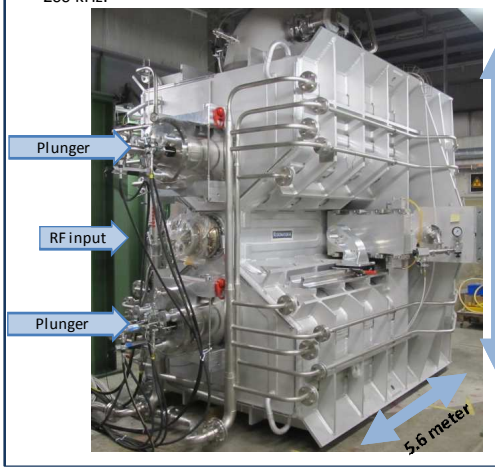
RF Interlock system

- Protects cavity and subsystems
- Based on a design for SwissFEL and SLS
- Manages local or remote operation



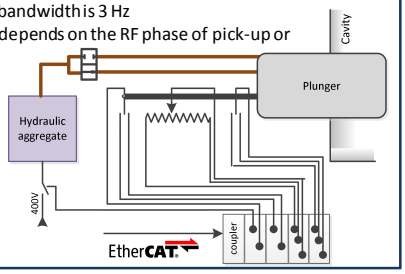
New Cavity for Injector 2

- The projected replacement of the 150MHz cavities with two new accelerating cavities at 50 MHz installed in Injector 2 triggered the upgrade of the LLRF systems. The normal-conducting aluminum cavities that are going to be installed have a Q of approx. 25'000 and are designed for an accelerating voltage of 400 kV.
- Two plungers are installed to tune the cavity in a range of approx. 200 kHz.



Cavity Tuning

- Symmetrical or differential operation
- Tuning system bandwidth is 3 Hz
- Feedback loop depends on the RF phase of pick-up or tuner position



Injector 2 upgrade described in: M. Bopp et al., *"Upgrade concepts of the PSI accelerator RF systems for a projected 3mA operation"*, Proc. 16th Int. Conf. on Cyclotrons and their Applications, East Lansing, 2001