The upgrade of J-PARC LINAC Low-Level Radio Frequency system

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Introduction

J-PARC (Japan Proton Accelerator Complex) LINAC was commissioned in October 2006. Its work is to accelerate an H^- beam with a peak current of 50mA and a pulse width of 500us up to 400MeV and then injected to Rapid Cycling Synchrotron (RCS). Up to present, the low level radio frequency control system of LINAC has been running for more than 10 years. Even it still works well, the supplier didn't produce the same products many years before, nor did they maintain. Besides this, according to the plan, the beam current of LINAC will increase to 60mA in recent months. As the result, the beam loading effect will be more serious, it puts forward a higher requirement for the performance of LLRF system. Considering these, a new LLRF system for J-PARC LINAC was developed and tested in the last few months. Its architecture and performance are presented.

System Architecture

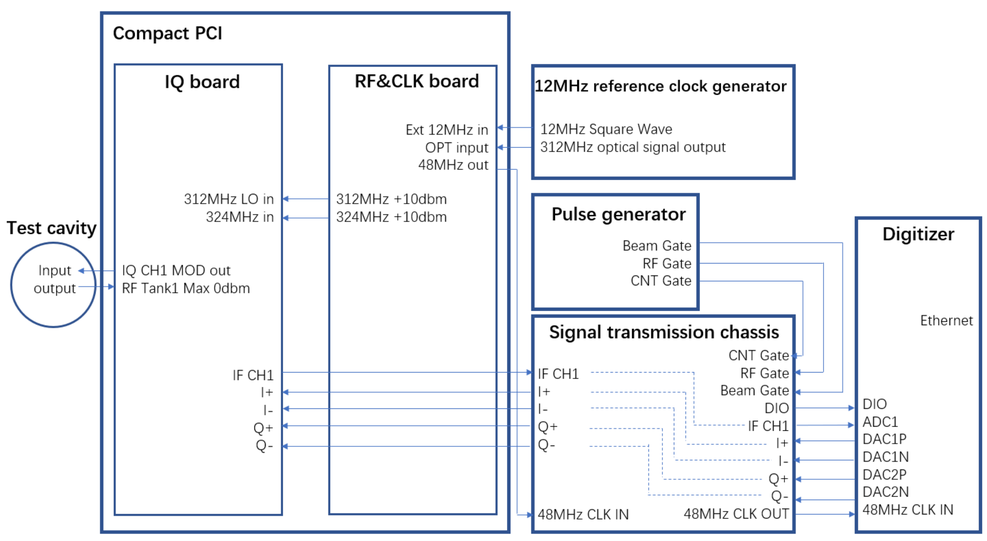

Fig 1. System Test Schematic Diagram

Fig 2. Low-level radio frequency control system

The new digitizer adopted MTCA.4 architecture. It includes 14 ADC, 2 DAC, 2 FPGA and optical communication connector. Both ADC and DAC are 16bits. The sampling speed of them are 80MSPS and 320MSPS (Million Samples per Second). In FMC (FPGA Mezzanine Card) board, Xilinx Spantan6 FPGA was used, which main tasks refer to IQ convert, amplitude and phase adjustment of ADC, vector-sum control and the control & monitoring of high-speed serial signal. Zynq 7000 FPGA was equipped in Carrier board. Its main function is to do the vector-sum control, filtering processing, feedforward & feedback control, PI control, amplitude and phase adjustment of DAC, EPICS input/output control (IOC) and the interlock criterion etc.

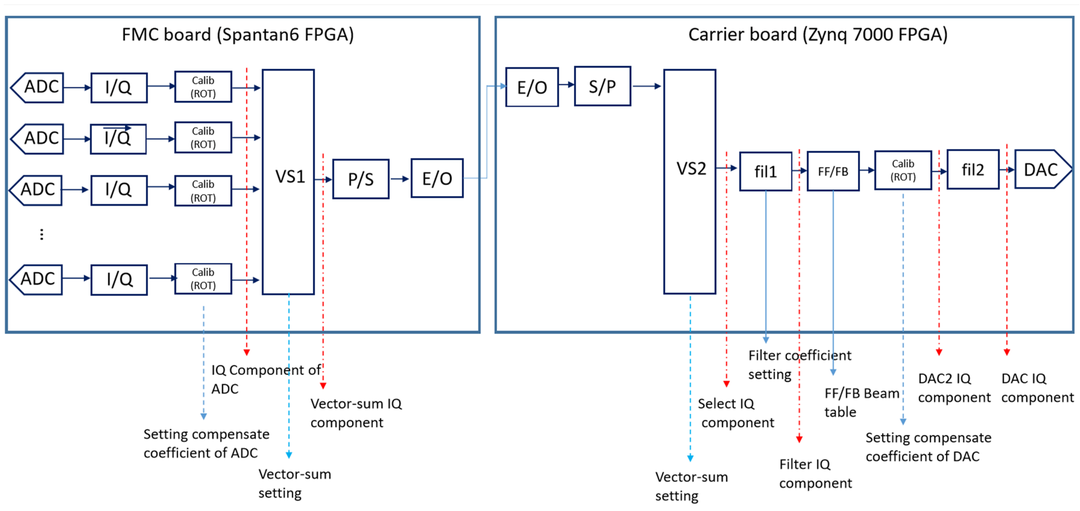

Fig. 3 FPGA signal flow diagram

System Performance

According to the control theory, the system transfer function for a open-loop system can be written as below,

$$H_{ol}(s) = \left(\frac{K_i K_p + K_p s}{s}\right) \cdot \left(\frac{w_{0.5}}{s + w_{0.5}}\right) \cdot e^{-\tau_d s} \cdot \left(\frac{w_f}{s + w_f}\right) \quad (1)$$

In our case, the Q factor of test cavity is 3664, half band width of cavity $w_{0.5}$ is $2.78 \times 10^5 rad/s$, system delay τ_d is 2.38usec, in which 2.11usec (delay from DAC to ADC outside FPGA) + 0.27usec (FPGA delay =13 clock cycle, 1 clock cycle = 1/48MHz). We didn't use filter, so w_f=0. In PI control, if we choose K_p=1, K_i=0, then equation (1) can be written as follow,

$$H_{ol}(s) = \left(\frac{2.78\times10^5}{s+2.78\times10^5}\right) \cdot e^{-2.38\times10^{-6}s} \quad (2)$$

From Bode plot we find that system is stable. And when we choose K_p=3, K_i=0 , we get the critical situation, shown as Fig 4. It means that K_p should be less than 3 when we do the PI value setting.

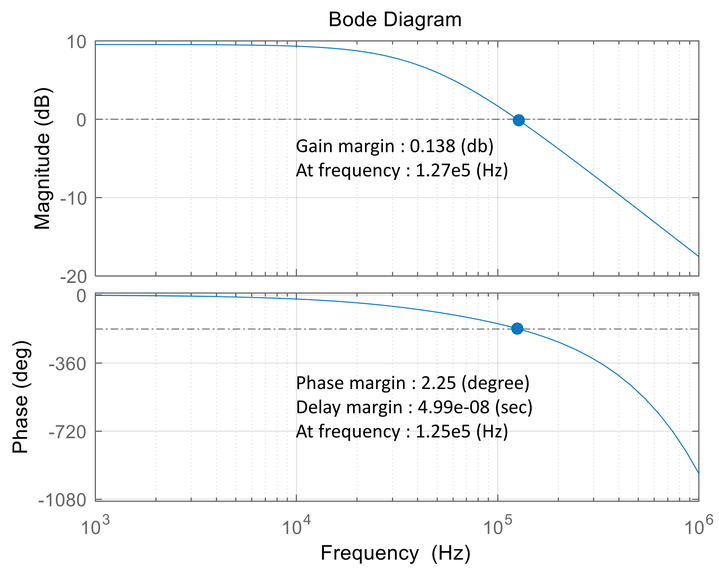

Fig. 4 Bode plot of system transfer function when K_p=3, K_i=0

For our system, P value set to 8 means actual K_p equals to 1. In practice operation, P value should not over 8, or it will cause oscillation. Figure below show the amplitude & phase stability of system when P value set to 5 and I value set to 2500 in real system. The amplitude stability is ±0.15%, phase stability is ±0.1°.

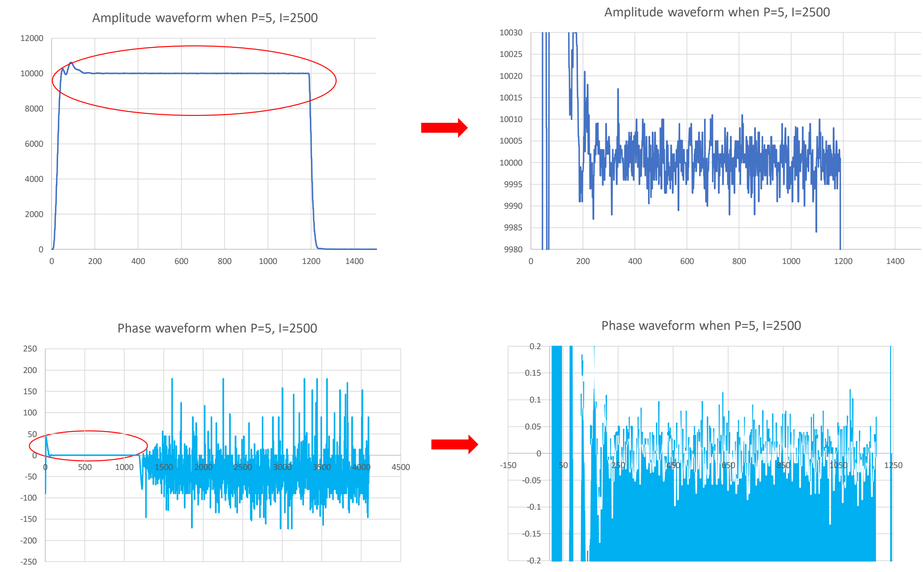

Fig. 5 Amplitude & Phase waveform when P value set to 5, I value set to 2500

Future Plan

In J-PARC, the cycle of chopped beam is 0.815usec, and the feed-forward waveform should be synchronizing with the chopping pulse, shown as Fig. 6. However, the rising-time of DAC that we measured is 3.66usec, shown as Fig. 7 . This value is too large to do the feedforward compensation. Additionally, in J-PARC one station just have one or two cavities, we don't need so many ADCs. For the future system, we wish to improve the performance of DAC and ADC, shorten their response time and rising-time. Moreover, current system still use CompactPCI crate and a signal transmission chassis. In the future, we want to integrate all of their function into the MicroTCA.4 chassis.

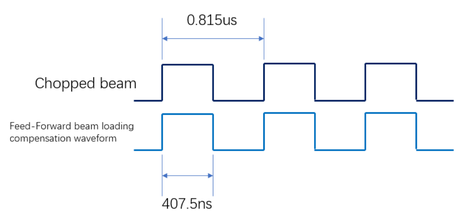

Fig. 6 Illustration of chopped beam and feed-forward compensation waveform

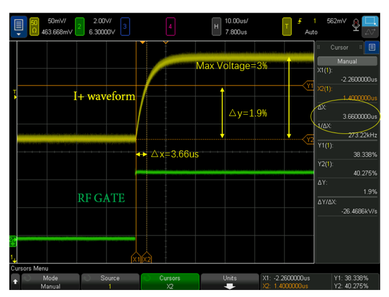

Fig. 7 DAC rising time