High Density Mixed Signal Hardware Design for Scientific Measurement and Control

SLAC NATIONAL ACCELERATOR LABORATORY

D. Van Winkle(dandvan@slac.Stanford.edu)

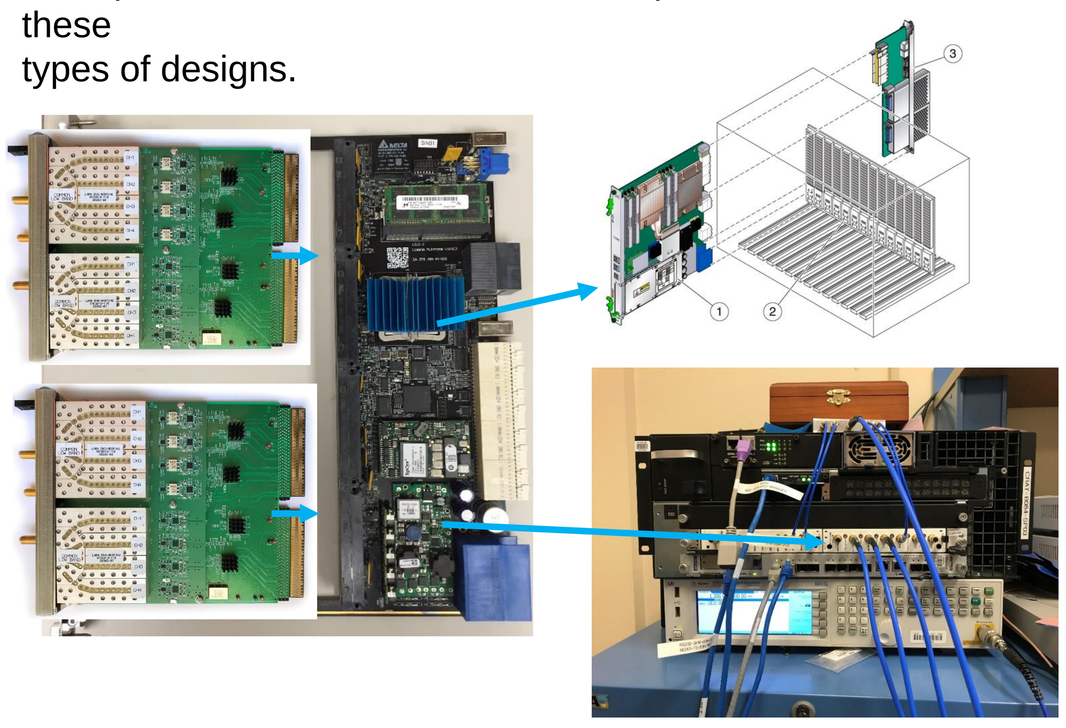
Abstract

The SLAC National Accelerator Laboratory has developed a new extensible platform based upon a common carrier in the industry standard Advanced Telecommunications Computing Architecture (ATCA) format. This new platform allows for a large variety of applications to be developed all within a standard (and modified standard) Advanced Mezzanine Card (AMC). Because this architecture is inherently compact, various mixed signal circuitry ends up being packed within a relatively small volume. This poster will highlight two of our high density designs (LLRF cards as well as 4 GHz 4000 channel receiver cards). We will show some key design techniques as well as potential pitfalls and present some results from our finished, operating cards.

ATCA Platform Description

The SLAC High Performance Architecture platform is an ATCA based system being designed at SLAC for almost all of the LCLS-II controls hardware (the exception being LLRF). To date over 20 boards have been developed for this platform for things ranging from BPM's to timing, to wire scanners to MPS. In addition, LLRF for Mission Readiness (upgrades to SLAC's original LINAC) have been developed and successfully run for over a year. Plans are in the work for a full sector install. SSRL is in the process of upgrading it's LLRF for the Booster and main ring using this modular architecture.

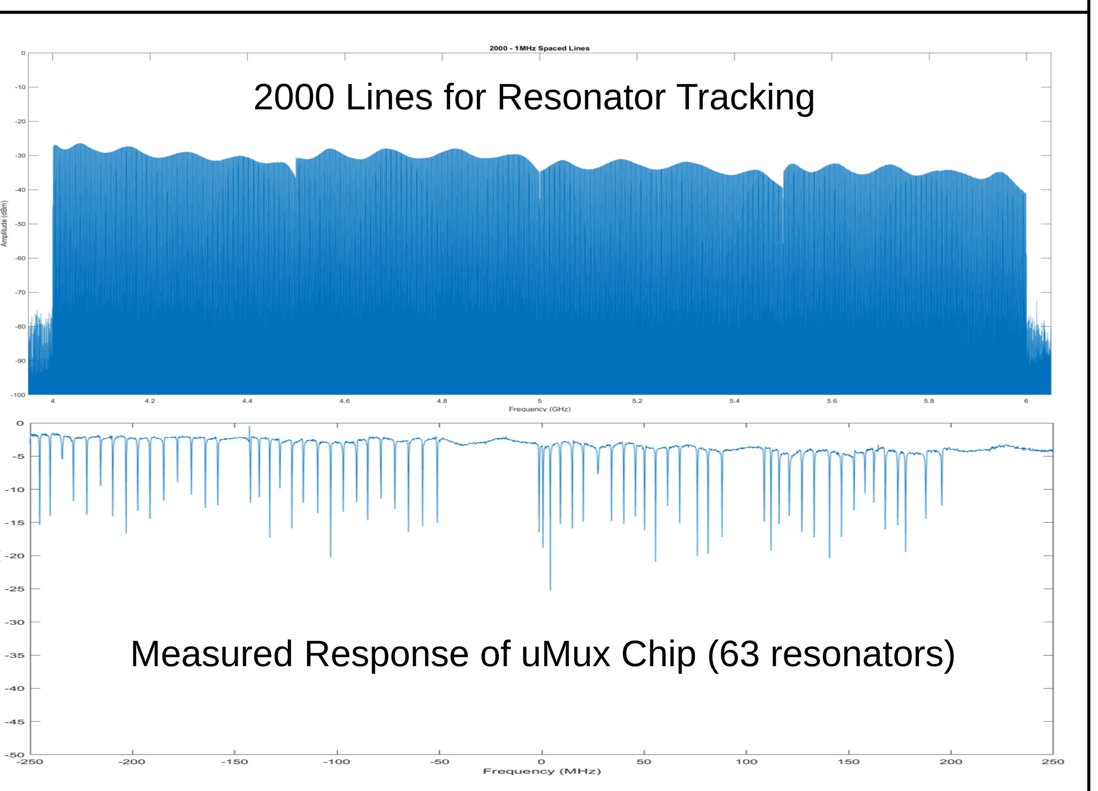
One of the main challenges of this system (which also apply to uTCA) is packing a lot of mixed signal circuitry into a tight space while trying to maintain good isolation and performance. This poster will discuss some of the challenges and techniques used to attempt to address some of the multiple issues associated with these
types of designs.



The heart of the system is the AMC carrier card. The carrier card is designed to take two double-wide AMC (Advanced Mezzanine Cards) which can be application specific. Key features of the carrier include:

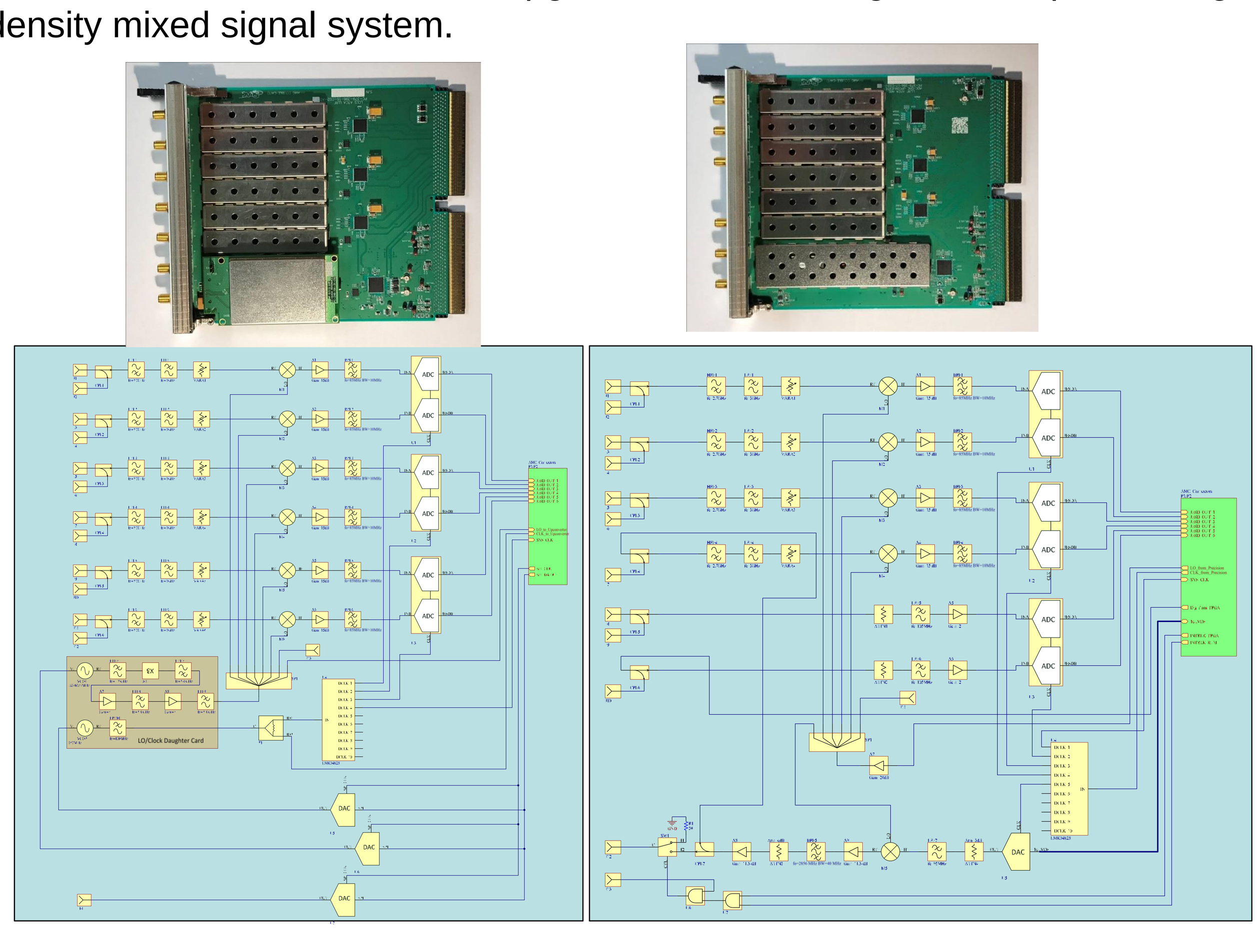
- Up to 10 12.5 GSPS JESD204B Rx Lanes (for ADCs for example)
- Up to 10 12.5 GSPS JESD204B Tx Landes (for DACs for example)
- 12V, 6V, 4V, 2V Managed Supplies
- Ethernet backplane support
- RTM connection for further low frequency IO
- Hot-swappable
- Multiple digitial IO
- Large Xilinx FPGA (XCKU060)
- Base Firmware with application space for AMC cards
- System Generator supported DSP development
- And more…

Some Results



Example AMC Designs

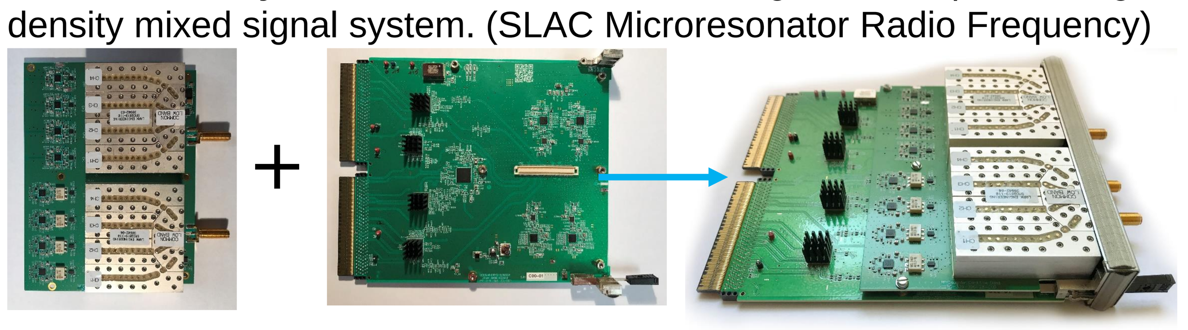
The **Mission Readiness LLRF** upgrade boards are a great example of a high density mixed signal system.

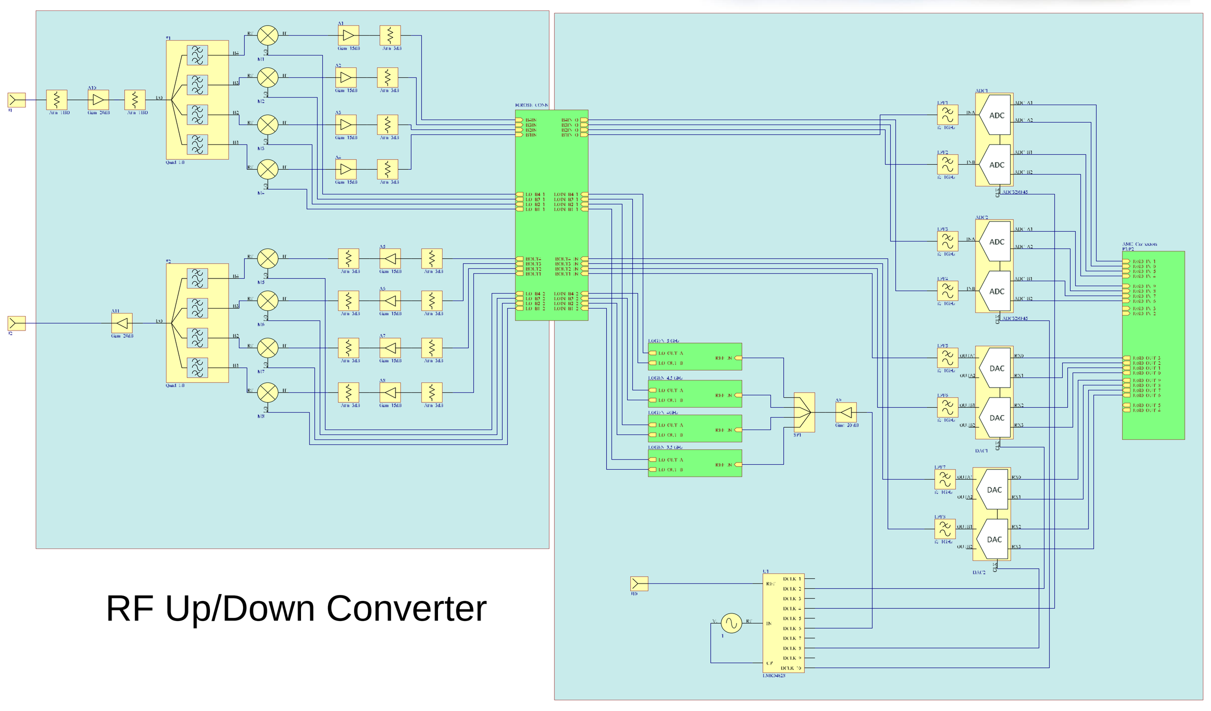


The board pair contains:

- 6 16-bit JESD204B ADC chips (12 ADCs clocked at 370 MHz)
- 1 16-bit Parallel DAC chip (clocked at 370 MHz)
- Onboard LO for 2856 MHz down/up conversion
- Onboard clock for 370 MHz clock routing
- Clock distribution chip
- 10 down-conversion channels
- 2 DC coupled channels
- 3 Slow DACs for LO locking and aux output

The **SMuRF Cryo Sensor** boards are another great example of a high density mixed signal system. (SLAC Microresonator Radio Frequency)





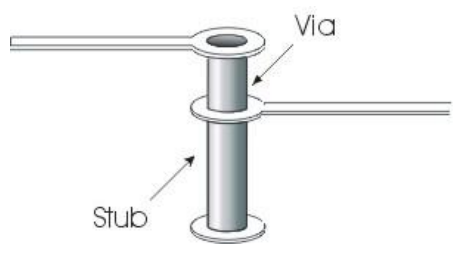
RF Up/Down Converter

SMuRF Base Board

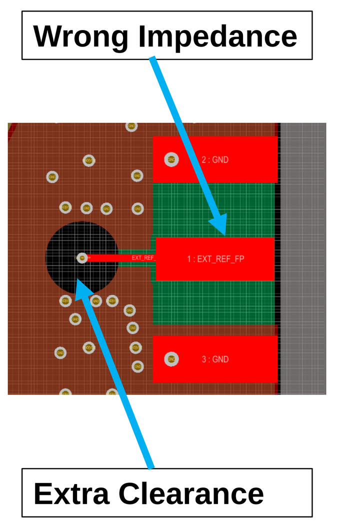
4 Bands of 500 MHz each are used to probe cryogenic resonators at ~300mK. Resonator spacing is planned for 1MHz for a total of 2000 tones coming out of this board. With two sets of boards covering the full 4-8 GHz range we are planning on 4000 tones total. These boards contain circuitry from DC to 8 GHz.

High Frequency Tips

At high frequencies, when going from say, GCPWG to strip-line on an inner layer, you can end up with a stub on the far side of the via. There are mitigations (back drilling or blind vias), but they can be expensive. Stubs can be radiative (hurting isolation), as well as affect the match across the transition. Pairs of stubs can couple well to each other (depending on frequency.

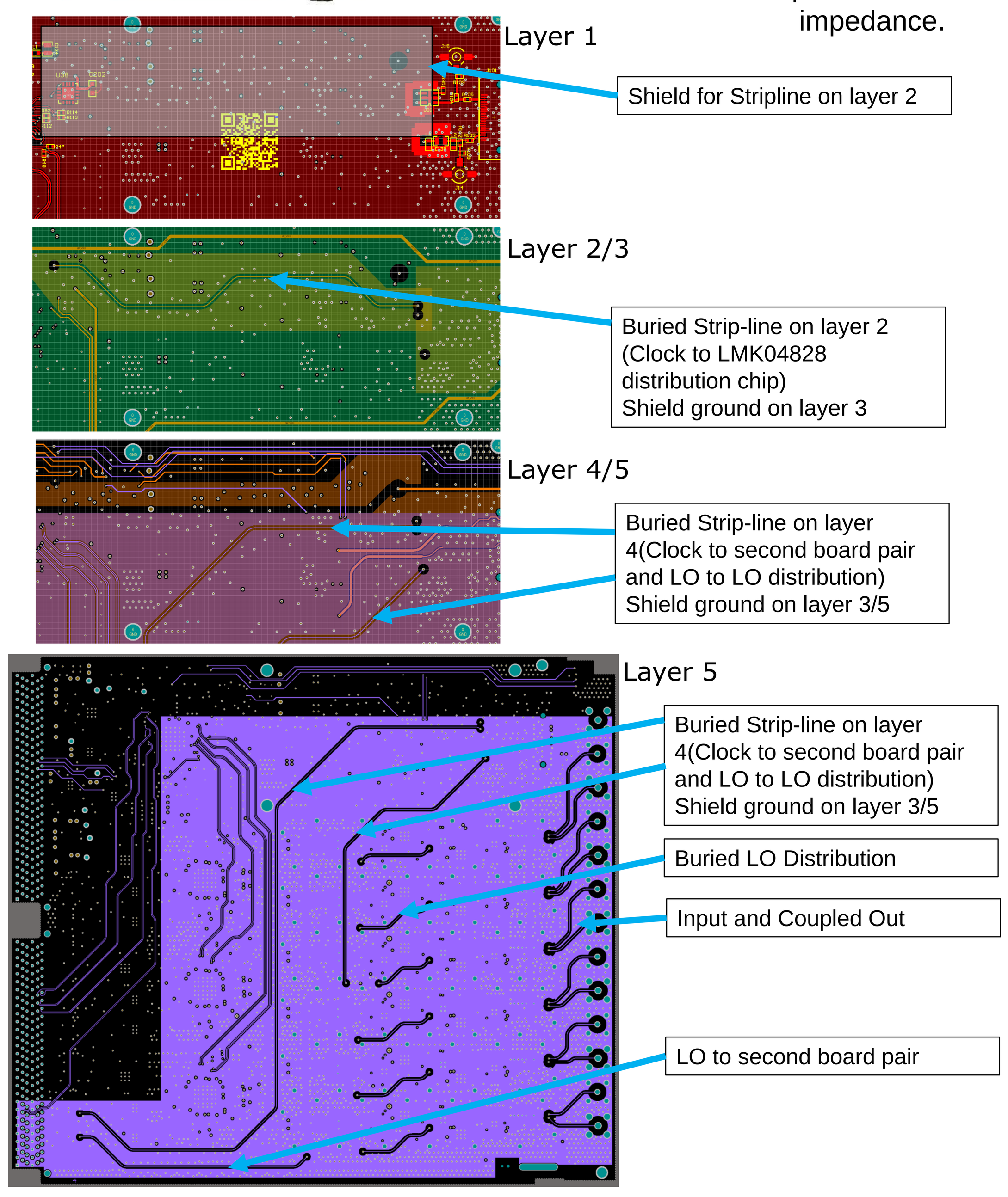


When transitioning RF to an inner layer, be sure to watch the impedance of the transition, standard via clearance is often not enough. Field solvers can be used to help design these transitions right the first time. Another thing to watch out for is wrong impedance on standard parts. This photo shows a very wrong impedance (around 20 ohms) resulted on the end launch SMA connector. The same thing can occur on part pads. If the part pad is bigger than the trace impedance you will end up with extra capacitance (or lower impedance) which can greatly impact your match.



Design Details

Grounding and shielding are obviously one of the most important aspects of any mixed signal design. My experience has shown that in general it is best to NOT split ground planes into digital and analog grounds unless you are EXTREMELY careful about crossing the ground domains. DC and low frequency return currents follow the path of least **resistance** whereas RF currents follow the path of least impedance.



SMuRF Challenges

One of the biggest challenges of the SMuRF electronics is the sheer number of signals that must be generated. Our scheme uses all of the following frequency ranges

- IF In/Out 500-1000 MHz
- RF Band 4-8 GHz in 8 500 MHz bands across two AMC boards
- JESD204B differential lanes running at 12.288 GHz
- Miscellaneous SPI Busses and digital logic at low frequencies.

The frequency planning hopefully allows us to run without interference due to the splitting of the frequencies.

Another big challenge of the SMuRF electronics is the linearity and noise requirements. Running 2000 tones through an amplifier at RF frequencies is challenging.

Conclusions

Modern accelerator and science controls are calling for more and more integration in smaller and smaller packages. With careful design and thinking "outside the BOX", it is possible to create high sensitivity solutions that meet even the most demanding applications.

These solutions are not without challenge and one of the big challenges has been running the extremely fast JESD204B lanes across connector interfaces and complicated boards.

With Xilinx introducing their new UltraScale+RFSoc product line, the issue of the JESD problem will quite possibly go away. Fortunately for us RF designers, we will still need to down/up-convert the IF signals to signals higher than these new products can currently generate and digitize.

The future looks bright for these type of mixed signal designs as chip vendors push their products higher and higher in frequency. It's unbelievable to this engineer how far things have come in his career.

Acknowledgments

The SMuRF crew including Sarah Stokes Kernasovskiy, Shawn Henderson, Steve Smith, Joe Frisch, John Dusatko, Mitch D'Ewart, Zeesh Ahmed, Dale Li, Dave Brown, Larry Ruckman and many more have been invaluable in making these projects a success.

In addition, many other have helped on the mission readiness LLRF including Dave Steele and Jim Sebek.

Work supported in part by Department of Energy contract DE-AC02-76SF00515