### Abstract

The SLAC National Accelerator Laboratory has developed a new prototype for a common carrier in the industry standard Advanced Telecommunications Computing Architecture (ATCA) format. This new platform allows for a large variety of applications to be developed all within a standard (and modified standard) Advanced Mezzanine Card (AMC). Because this architecture is inherently compact, various mixed signal circuitry ends up being packed within a relatively small volume. This poster will highlight two of our high density designs (LLRF cards as well as a 4 GHz 4000 channel receiver cards). We will show some key design techniques as well as potential pitfalls and present some results from our finished, operating cards.

### Design Details

Grounding and shielding are obviously one of the most important aspects of any mixed signal design. My experience has shown that in general it is best to NOT split ground planes into digital and analog grounds unless you are EXTREMELY careful about crossing the ground domains. DC and low frequency return currents follow the path of least resistance whereas RF currents follow the path of least impedance.

#### SMuRF Challenges

One of the biggest challenges of the SMuRF electronics is the sheer number of signals that must be generated. Our scheme uses all of the following frequency ranges

- IF In/Out 500-1000 MHz
- RF Band 4-8 GHz in 8 500 MHz bands across two AMC boards
- JESD204B differential lanes running at 12.288 GHz
- Miscellaneous SPI Busses and digital log at low frequencies

The frequency planning hopefully allows us to run without interference due to the splitting of the frequencies.

Another big challenge of the SMuRF electronics is the linearity and noise requirements. Running 2000 tones through an amplifier at RF frequencies is challenging.

### Conclusions

Modern accelerator and science controls are calling for more and more automation in smaller and smaller packages. With careful design and thinking 'outside the BOX', it is possible to create high sensitivity solutions that meet even the most demanding applications.

These solutions are not without challenge and one of the big challenges has been running the extremely fast JESD204B lanes across connector interfaces and complicated boards.

With Xilinx introducing their new UltraScale+RFSoC product line, the issue of the JESD problem will quite possibly go away. Fortunately for us RF designers, we will still need to down/convert the IF signals to signals higher than these new products can currently generate and digitize.

The future looks bright for these type of mixed signal designs as chip vendors push their products higher and higher in frequency. It’s unbelievable to this engineer how far things have come in his career.

### Acknowledgments

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### Example AMC Designs

The Mission Readiness LLRF upgrade boards are a great example of a high density mixed signal system.

- **The board pair contains:**
  - 6 16-bit JESD204B ADC chips (12 ADCs clocked at 370 MHz)
  - 1 16-bit Parallel DAC chip (clocked at 370 MHz)
  - Onboard LO for 2856 MHz down/up conversion
  - Onboard clock for 370 MHz clock routing
  - Clock distribution chip
  - 10 down-conversion channels
  - 2 DC coupled channels
  - 3 Slow DACs for LO locking and aux output

- **The SMuRF Cryo Sensor** boards are another great example of a high density mixed signal system (SLAC Microresonator Radio Frequency)

### High Frequency Tips

At high frequencies, when going from say, GCPWG to on the line on an inner layer, you can end up with a stub on the far side of the via. There are mitigations (back drilling or blind vias), but they can be expensive. Stubs can be radiative (hurting isolation), as well as affect the match across the transition. Pairs of stubs can couple well to each other (depending on frequency).

When transitioning RF to an inner layer, be sure to watch the impedance of the transition, standard via clearance is often not enough. Field solvers can be used to help design these transitions right the first time. Another thing to watch out for is wrong impedance on standard parts. This photo shows a very wrong impedance (around 200 ohms) resulted on the end launch SMA connector. The same thing can occur on part pads. If the part pad is bigger than the trace impedance you will end up with extra capacitance (or lower impedance) which can greatly impact your match.

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### Some Results

- **2000 Lines for Resonator Tracking**
  - Measured Response of dMux Chip (63 resonators)