FRIB LLRF Control: Issues and Improvements

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Tuner Control

Stepper

Problem: During the ReA6 2 cavity cryo-module 24 hour test, original stepper/piezo driver board stopped driving causing trips.

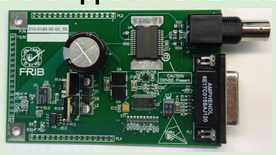
Root cause: Small chip package handles several watt power without proper heat management, eventually overheated.

Solution: Copper pour and heat sinks were added on both sides of the PCB.

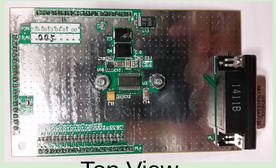
Since the micro-stepping feature of the stepper driver is verified, piezo driver is removed.

	ReA6	High Speed	Low Speed	Trinamic
Accel Current (A)	1.36	1.57	2.37	1.3
Run Current (A)	2.04	2.37	1.57	1.0
Holding Current (A)	0.44	0.51	0.51	0.4
Run Condition	< 50%	Continuous	Continuous	Tuning Range Test
Test Time (hrs)	24	17	25	< 1

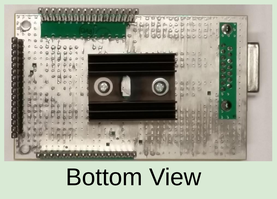
Old Stepper/Piezo Board



New Stepper Only Board



Top View



Bottom View

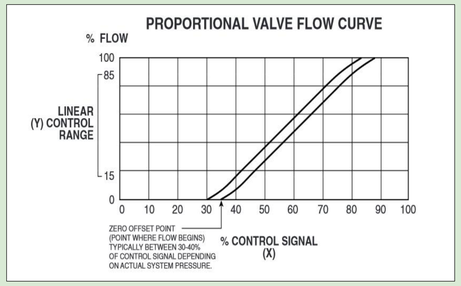
Pneumatic

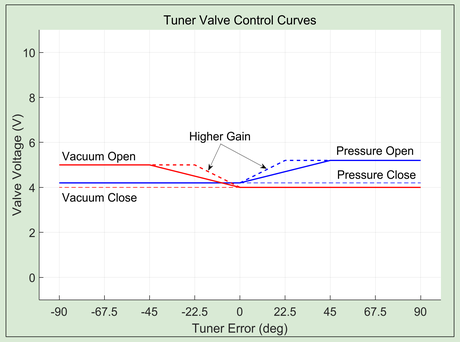
Analog tuner board provides two 0 ~ 5 V analog output channels to control the pressure and vacuum valves for the tuner manifold.

Valve calibration procedure based on ANL procedure:

Dead-zone calibration:
- Set pressure valve close voltage so that pressure increase at *0.001 - 0.002* psi/sec rate;
- Set vacuum valve close voltage so that pressure is stable;

Maximum tuning speed setting:
- Set pressure valve open voltage so that pressure increase at *0.2 - 0.3* psi/sec rate;
- Set vacuum valve open voltage so that pressure decrease at *0.2 - 0.3* psi/sec rate.





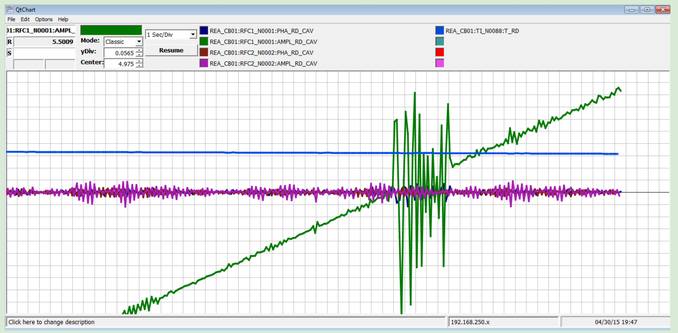
RF Control

Internal Variable Overflow

Problem: During the ReA6 2 cavity cryo-module 24 hour test, amplitude control was found not stable at certain set-points during ramp up.

Root cause: Amplitude control loop Internal variable overflows.

Solution: Control algorithm was optimized with proper scaling.

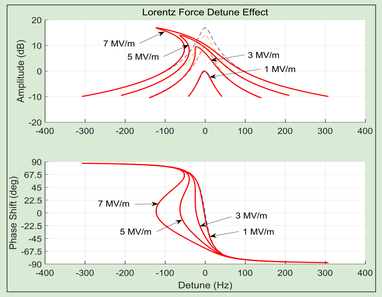


Lorenz Force Detuning (LFD)

Problem: During the HWR53 integrated test, it was hard to lock the cavity.

Root cause: Significant LFD effects at high field.

Solution: Good amplitude regulation is critical to minimize LFD effect; slower ramp rate help keeping cavity locked.



Smooth Switching between Open and Close Loop

Problem: In some of the tests, it was found that when closing the RF control loop, the system with trip.

Root cause: Sudden control effort change causes trip events.

Solution: Smooth switch was implemented in the control algorithm.

Design Changes

Remove one Digital to Analog Converter (DAC)
- Cost reduction (trade one RF switch for one DAC)
- Free 29 input/output pins

Remove analog board
- Remove one FPGA (Spartan 3E), less firmware to maintain
- Easier installation

Add EEPROM to RF board
- Device calibration data can be stored local for easy swap

Address the LLC interlock false trigger issue
- Add capacitor to filter noise on 24 V signal provided by the low level control PLC
- Add opto-isolator to the AMP_STATUS signal
- Layout changes to reduce crosstalk

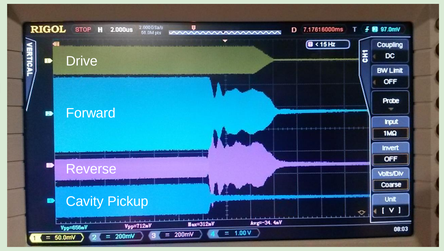
Add RF output feedback path to spare input channel
- Reboot phase calibration

Add chassis fan/filter
- *Better cooling, reduce dust accumulation*

Interlocks for RFQ Conditioning

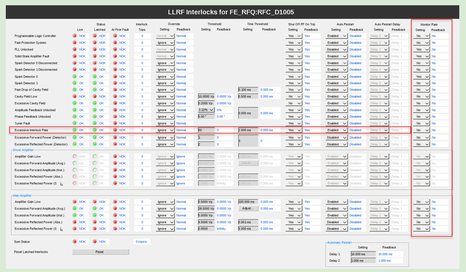
Quick shut off time

To protect RFQ from damage due to driving high power into the cavity when a spark happens, a fast interlock was implemented to turn off RF in less than 5 microseconds.



Interlock Rate Interlock

The user can select a set of interlocks of interest to be monitored for high interlock rate. If the number of interlocks happen in a defined time window exceeds the threshold, the interlock rate interlock will trigger.



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