TRIUMF

Canada's national laboratory for particle and nuclear physics
Laboratoire national canadien pour la recherche en physique nucléaire et en physique des particules

DSP Implementation of an Iterative Learning Controller

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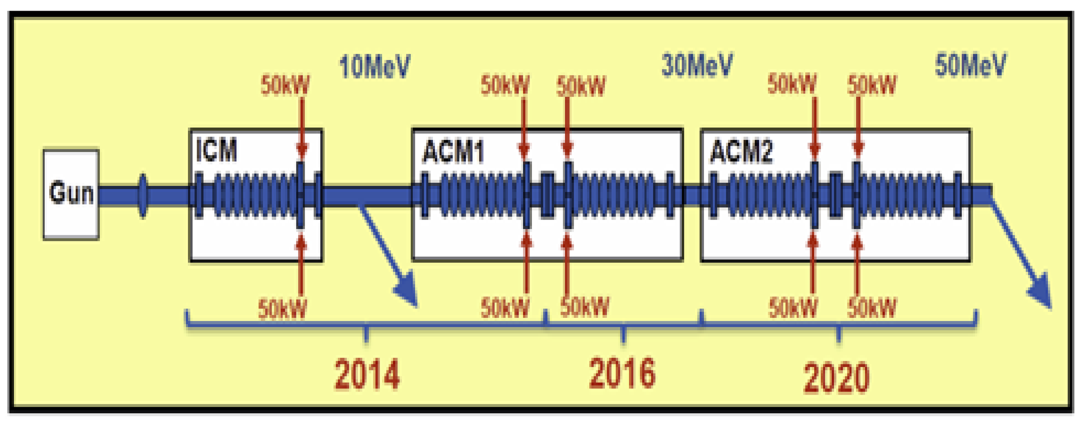
Abstract

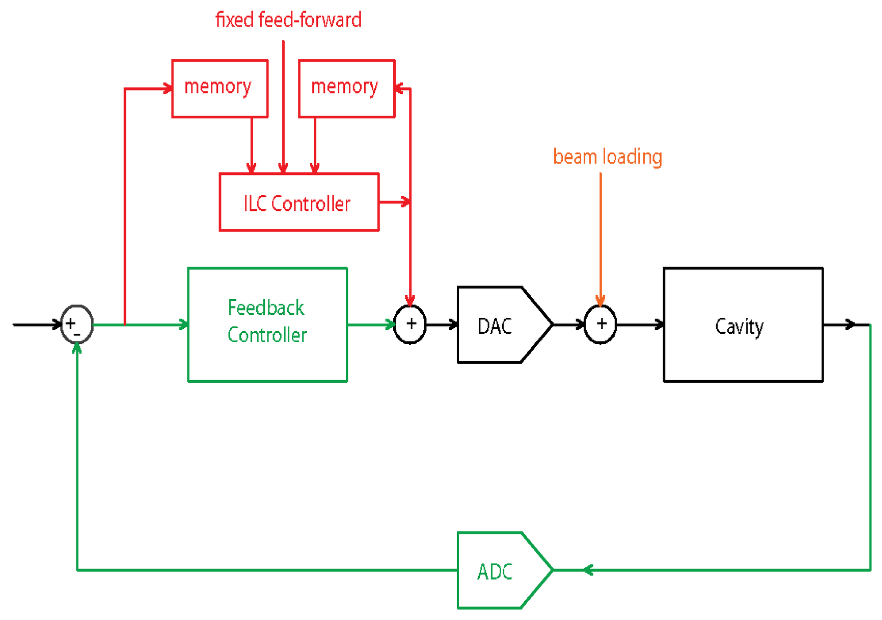
An iterative learning controller is a type of adaptive feed-forward. In this case it has been developed to control the expected high beam loading of the TRIUMF electron linac. Some of the details of the design process are outlined, beginning with the feasibility of adding such a controller to the existing digital signal processor, which currently implements PID control of the cavity amplitude and phase. The method by which the ILC was implemented, the costs in terms of processing overhead, and some early test results are described.

TRIUMF e-Linac



- 300 KV electron gun, 10 mA CW, 650 MHz
- Dielectric waveguide to bring RF to gun
- Injector Cryomodule – 9-cell cavity @1.3 GHz
- Accelerator Cryomodules – 2 9-cell cavities each, driven by a single klystron
- Each cavity adds 10MeV for a total of 50 MeV or 0.5 MW of beam power

Iterative Learning Controller



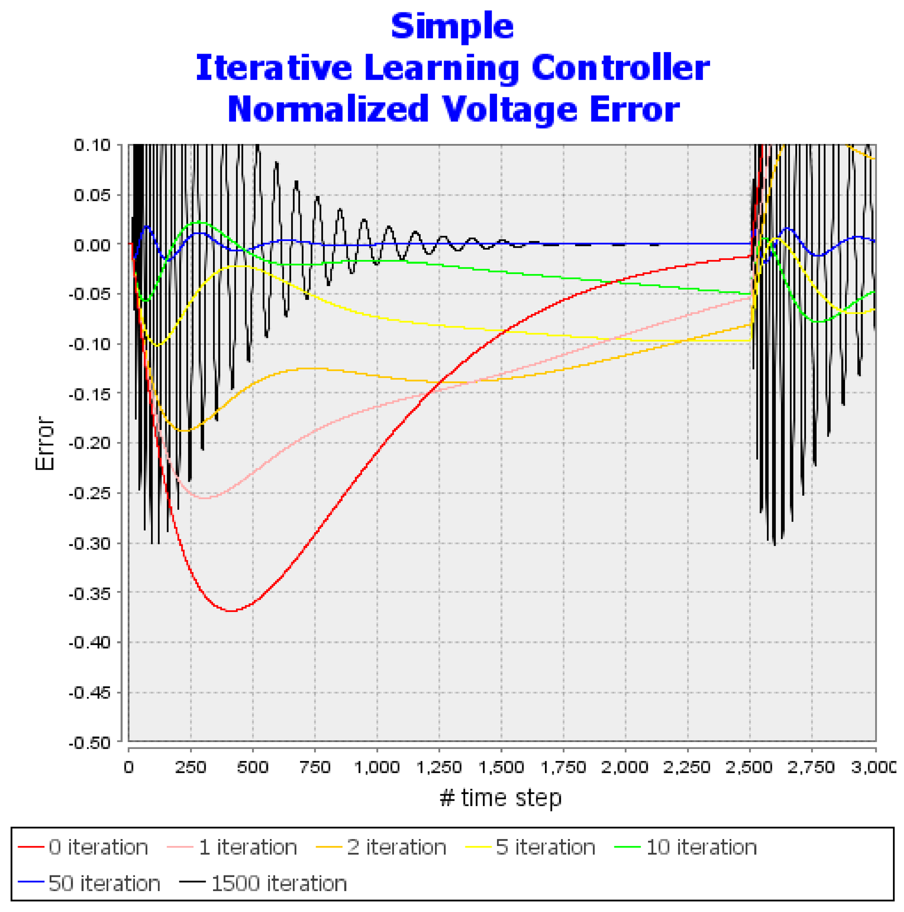
- Conventional PID controller with ILC controller/memory added
- Beam-loading effect is repetitive pulse-pulse
- Previous correction + error term used to construct current correction
- Cannot correct pulse-pulse variation, cavity microphonics, or amplifier drive fluctuation (conventional PID still required)
- Non-causal ILC :

$$u_{k+1}(T) = u_k(T) + \frac{1}{3}\left[e_k(T+1) + e_k(T+2) + e_k(T+3)\right]$$

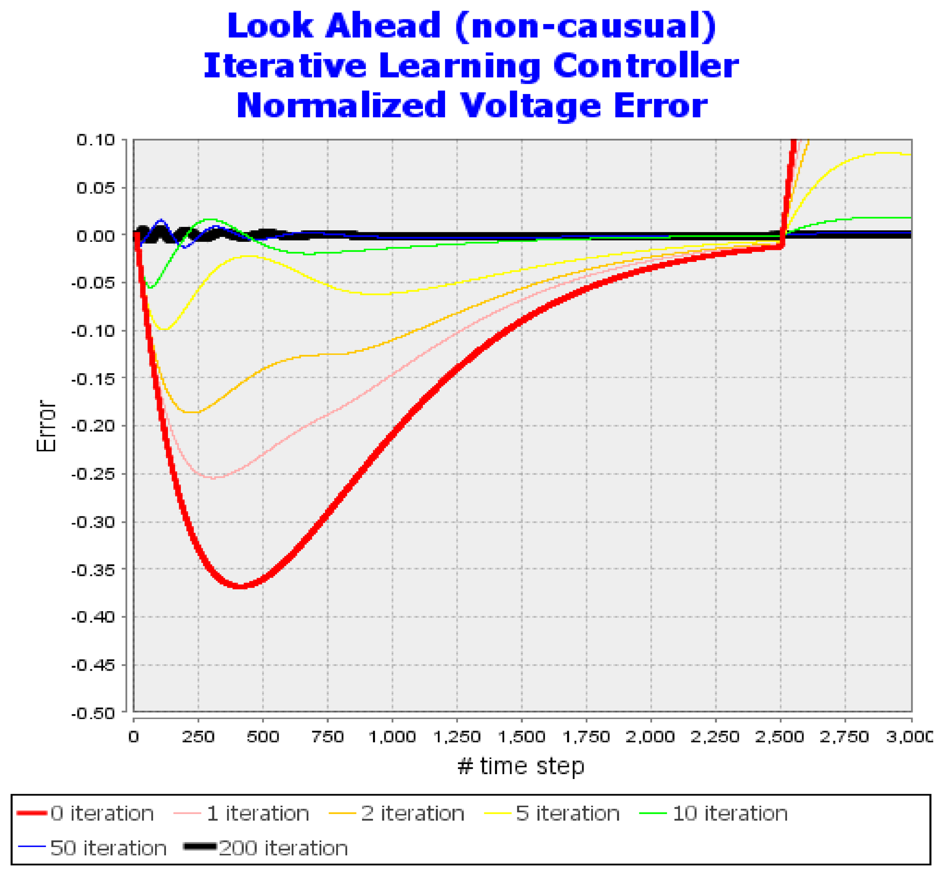
Feasibility

- Proposed algorithm was examined to determine feasibility of incorporation into existing DSP-based PID controller
- 2 memory buffers required – one already present as part of PID algorithm (3 consecutive error samples)
- Second buffer used to store data from previous pulses – minimum size = pulse period/loop sample time ~ 500 samples maximum
- To meet above requirement and avoid overflow of circular buffers, 1k buffers were implemented. These easily fit into the available 2k on chip memories
- All on chip registers currently in use, implementing additional buffers would require register sharing between tasks
- Implementing ILC would require additional processing time and slow the sampling loop, but loop bandwidth still much lower (~1000x) than sampling frequency

Simulation Results



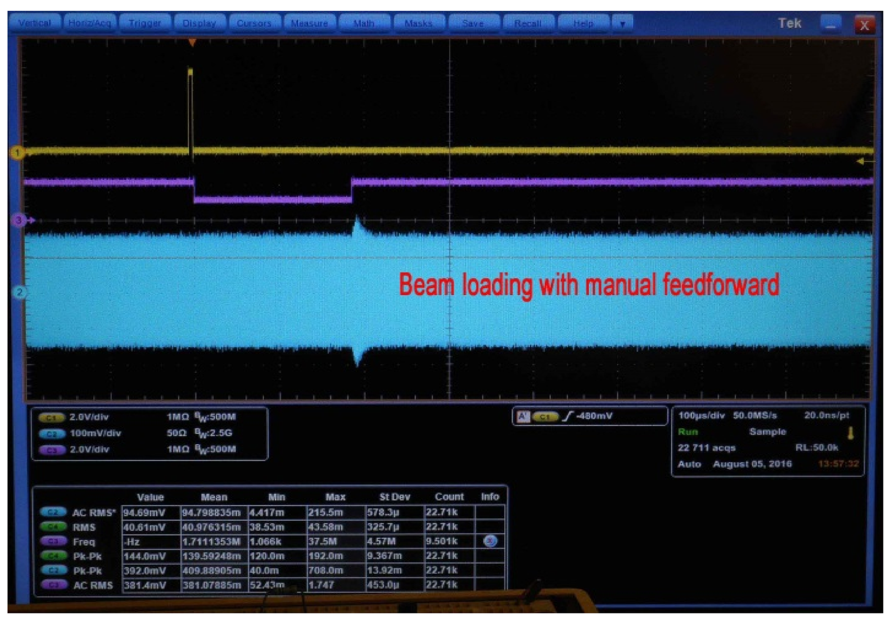
Non-Causal ILC Error

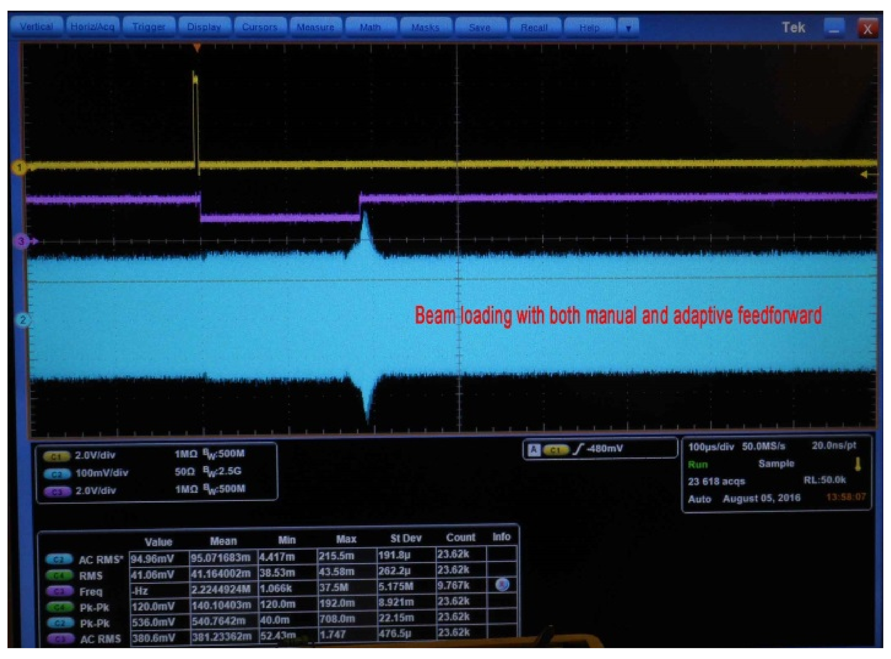


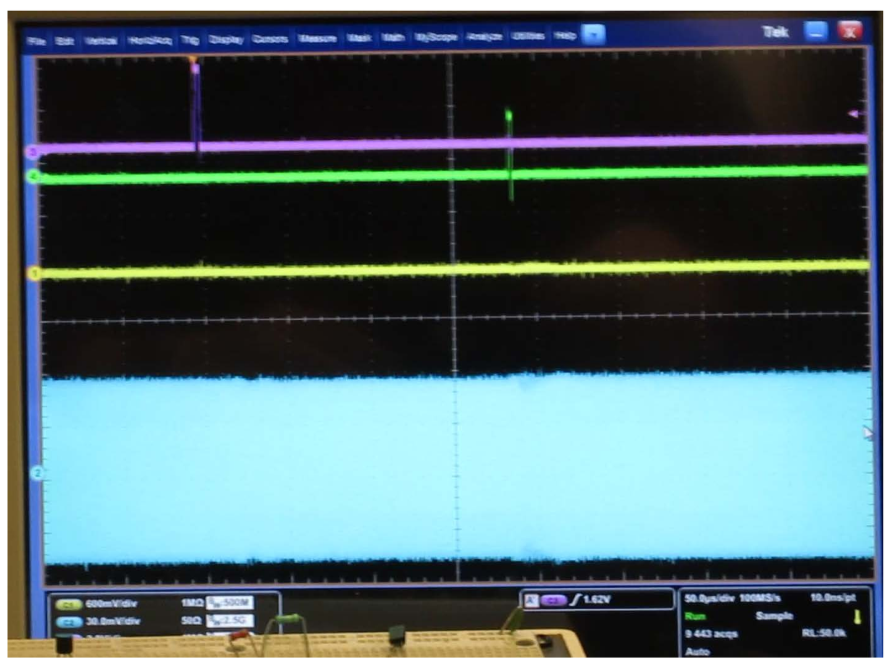
Causal ILC Error

Implementation/test results

- DSP-based implementation
- 320k samples/sec, pulse rate 1 kHz > 320 samples/pulse
- ILC overhead – total lines of code 1240 -> 1566 and loop code 110 -> 158 instructions for about a 30% reduction in sampling rate – still more than adequate
- Look-ahead had to be increased from 1 to 2 sample times because sampling is not synchronized to beam pulse
- Fixed correction (for given beam) + variable ILC correction
- ILC response speed also made a variable parameter
- System was tested on a normal conducting cavity with simulated beam loading







ILC System Response

Conclusion

- Causal ILC system is unstable (double integration involved)
- Non-causal system - stable + converges rapidly
- Overhead due to ILC implementation of ~30% is not enough to measurably impact control bandwidth
- Work done to control voltage transient at end of pulse – delayed end of feedforward control by ~8 samples
- Testing on superconducting cavity remains to be done