EPICS and VHDL developments in the LLRF for MYRRHA project's RFQ prototype.

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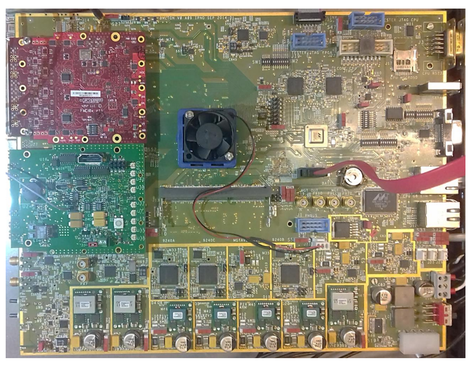
Abstract

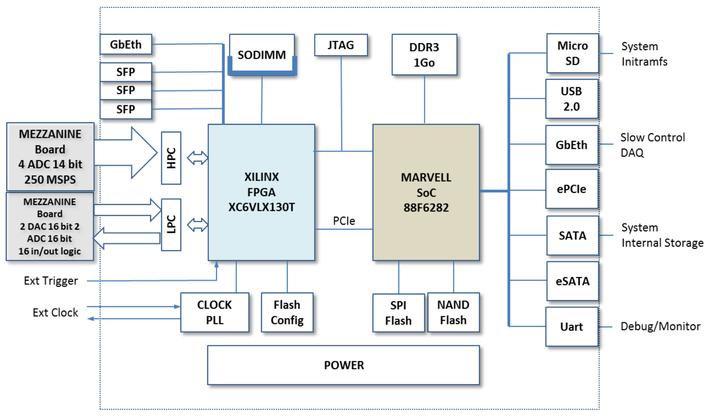
The European MYRTE project (for MYRRHA Research and Transmutation Endeavour), that aims to perform research and development work for supporting MYRRHA facility's development, is mainly focused on Accelerator R&D for ADS/MYRRHA WorkPackage (WP2) : the injector demonstrator. In this context, a control and command system is in development at IPNO, by merging both FPGA and EPICS software technologies, for the MYRRHA RFQ low level radio frequency (LLRF) to be produced at IPNO. This work is supported by the European Atomic Energy Community's (Euratom) H2020 Program me under grant agreement n°662186186 (MYRTE Project).

Actually, the EPICS platform (Experimental Physics and Industrial Control System) is an efficient tool to design input/output controllers (IOCs) to achieve control, command and supervision applications. On the other hand, FPGA components also provide a relevant hardware solution for control of systems. The control and command workstation in development at IPNO includes : a VHDL code embedded inside the FPGA to achieve regulation and signal processing tasks, a complete PCIe driver that ensure communications between the FPGA and the EPICS IOC, this one managing a Process Variables database and a channel access server to communicate with remote client applications. Work at IPNO also includes the design of a CSS - BOY (Control System Studio - Best OPI Yet) client supervision application.

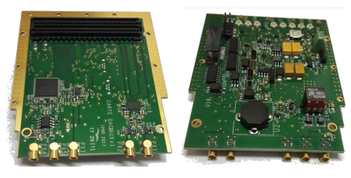
This poster presents both EPICS and VHDL developments for the IPNO LLRF, from the hardware data processing (FPGA part) to the outside communication and database management with the use of an embedded IOC in the LLRF. For a detailed description of the MYRRHA RFQ's LLRF, see poster P-54 : ***LLRF for the RFQ prototype of the MYRRHA project***.

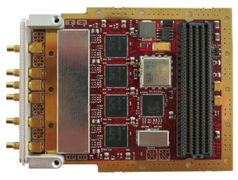
Architecture of the Dalton board



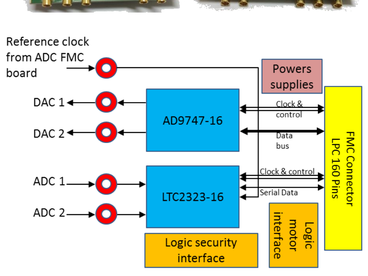


The DALTON motherboard board, developed at IPNO, is an in-house hardware solution to perform the control command and signal processing for the LLRF. It is equipped with a Xilinx Virtex 6 FPGA and a Marvell 88F6282 processor (ARM v-5 based), connected to each other with a PCIe bus.

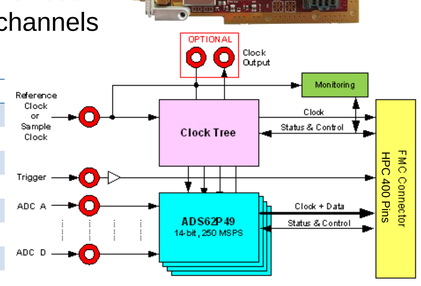




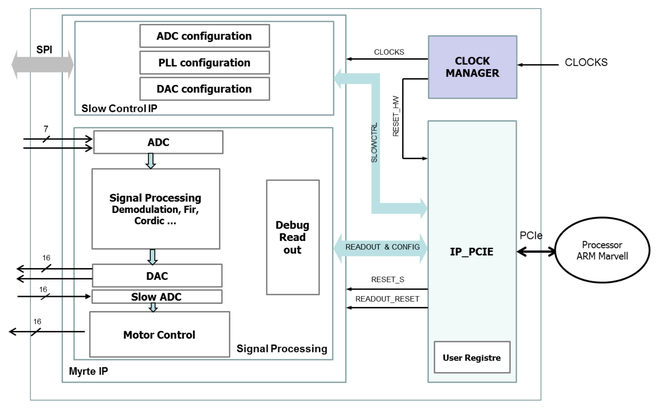
Two mezzanine board are connected to the DALTON board : an ADC FMC board 4DSP (FMC104) with 4 channels (right) and an in-house DAC&AUX board (left). For the latter, logic inputs have been validated, while ADC and DAC channels are currently tested at IPNO.



FMC104 Parameters	
Nb of channels	4
Resolution [bit]	14
Input range [Volt]	2V p-p (10dBm)
Input bandwidth [MHz]	3 to 650 (AC-coupled)
Input impedance [Ω]	50
SNR@10MHz [dBFS]	79
SFDR@10MHz [dBc]	77
Sampling [MSPS]	250 max



VHDL developments for the Xilinx Virtex 6 FPGA

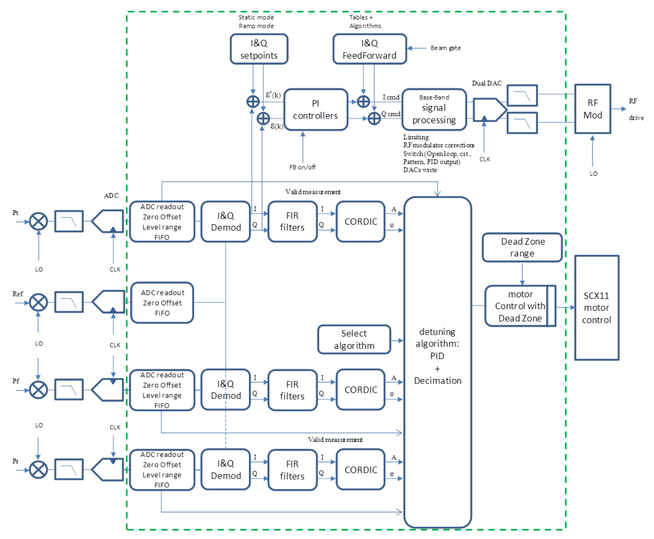


The VHDL architecture has three main parts.

The first one is a PCIe communication IP that allows the FPGA to communicate with the processor.

The second one is a slow control IP, to configure the hardware directly connected to the mother board.

The purpose of the last part is to manage signal processing: this is done using dedicated modules for each operation (IQ demodulation, filtering, CORDIC algorithm, etc…).



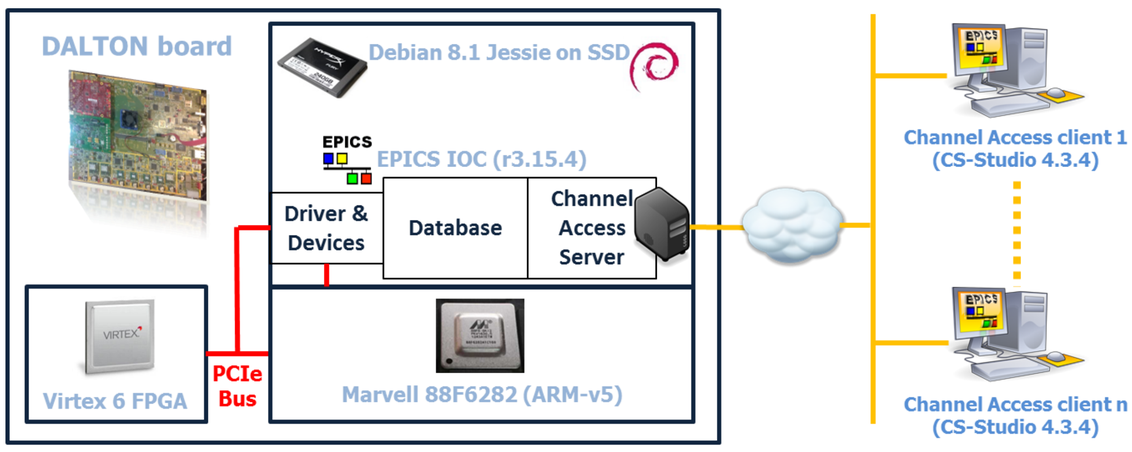
Current VHDL developments stand in the green box. In a word, FPGA's signal processing provides inputs signals for two main loops.

The first one is a PI loop for the RFQ's cavity field amplitude and phase regulation; it works with I/Q input signals.

The second loop is a PID one that regulates the RFQ's frequency with a motorized tuner.

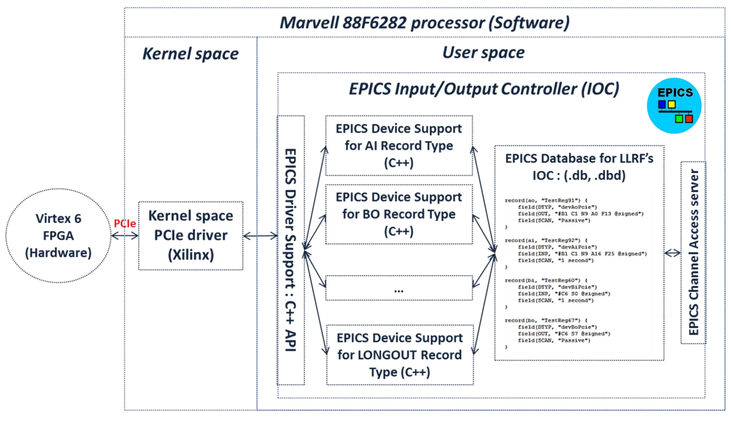
Future additions to the hardware architecture include a feed forward functionality, and a numerical self-exacting loop (SEL). For now, an analogic SEL is used for tests. An EPICS IOC has already been fully developed and tested for this sub-system.

The EPICS I/O Controller



To perform the LLRF's control system, an EPICS I/O Controller (IOC) communicates with the FPGA. A PCIe bus drives data exchanges between the IOC and the hardware.

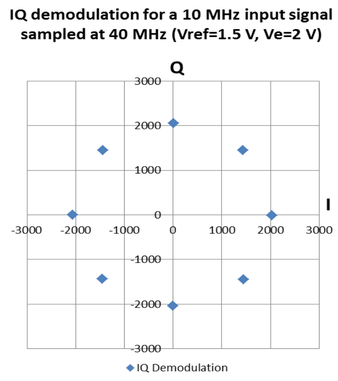
The EPICS relational database (PVs) interacts both with the hardware (system calls, DMA …) and a channel access server. The latter is the interface with remote client applications that manage control and monitoring tasks.



An in-house PCIe Linux kernel driver performs the communication with the FPGA. The driver layer of the IOC is a C++ API to wrap system calls and DMA and store hardware data. Then a device layer provides primitives to redirect inputs to the Process Variables, or to apply commands to the hardware. The Channel Access Server is the link with the outside.

Preliminary Results

Except for predistorsion module and calibration, signal processing in the FPGA has been developed and tested. VHDL main remaining developments include the DAC implementation, the motor control, and also safety and debug-related modules.

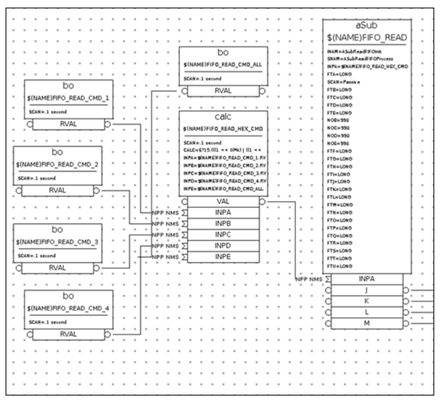


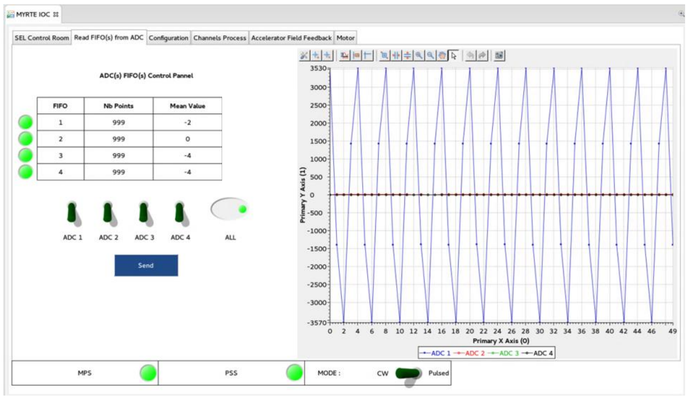
Phase [DEG]	$\frac{A_{stddev}}{A_{mean}}$ [%]	Phase Std dev [DEG]
0	0.079	0.036
45	0.056	0.037
90	0.071	0.038
135	0.062	0.041
180	0.069	0.041
225	0.066	0.032
270	0.056	0.037
315	0.069	0.033

IQ Demodulation : ADCs tests with arbitrary functions generator AGF3102; better results are expected with the use of the master oscillator, see poster 54.

The EPICS relational database provides a large set of Process Variables to control the whole LLRF. Each sub-system has its associated database and OPI, to increase modularity and stability for the global system.

A first version of database has been successfully linked to the hardware. The complete definition of each PV (and each field inside it) is in progress. OPIs for input signals setups (ADCs) and monitoring are fully operational, while others need to be tested at the same time as hardware developments.





Conclusion and Perspectives

The presented developments aim to produce a complete LLRF's control architecture. For now, the VHDL code for nearly all of the signal processing is finished. EPICS developments lead to a first version for both the IOC and the PVs database. The test phase is currently in progress, with software developments being validated at the same time as the hardware's. The objective is to design a complete LLRF by the end of 2017, to get ready for the MYRTE RFQ's test in 2018. For MYRRHA's final accelerator, a hardware evolution to the µTCA standard is planned, both for better reliability and software stability.