ApplicationCore: A Framework for Modern Control Applications at the Example of a Facility Independent LLRF Server

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Motivation

- MicroTCA-based LLRF system developed by DESY used in many facilities: FLASH, EuropeanXFEL and REGAE at DESY, ELBE at HZDR, FLUTE at KIT, TARA at Ankara University (and more to come!)
- Facilities use different control system middleware: DOOCS at DESY, Siemens Simatic/WinCC with OPC UA at ELBE, EPICS 3 at FLUTE, EPICS 4 at TARA
- IF control loop running in FPGA requires relatively complicated software interface providing many control tables etc.
- ~ 700 control system variables for the single cavity controller, ~ 3000 variables for the vector sum controller
- Contains some complex algorithms (e.g. adaptive feed forward)
- Porting to different control systems by branching would be difficult to maintain
- Adaptation for different DOOCS-based systems at DESY already creates many problems: improve on modularity!

ChimeraTK abstraction layers

- DeviceAccess allows access to devices with different transport protocols
- ControlSystemAdapter allows to write applications for different middlewares
- ApplicationCore unifies both, and adds modularity and multi-threading

Concept of ApplicationCore

- Application consists of many modules: application modules with use code (algorithms), device modules and control system modules
- Main application part instantiates modules and defines connections

Application modules

- Have input and output “accessors”
- Accessors are same as in Device/Access:
  - can be used like normal variables
  - can be scalar or arrays of any fundamental data type
  - functions like read()/write() trigger data transfer
- Each application module has a threaded running user code

Update mode and trigger

- Each accessor must be defined either push or poll
- Triggers can be used to initiate data transfer e.g. from poll-only devices (not sending interrupts)
- Any push-type data source can be used as trigger
- LLRF server: use macro pulse number from timing system as trigger for readback from FPGA

Variables groups

- Can be grouped for improved structure
- Group-wide trashes possible in owning thread: writeAll(), readAll(), readByKey() etc.
- In description of connections, groups can be connected with a single command: connectTo()

Multi-threading

- Modern inter-thread communication and synchronisation based on queues and futures
- This is build into ApplicationCore, no need to deal with it in user code!
- Application modules just use their inputs and outputs, which will be connected automatically with queues
- Synchronisation works by means of blocking calls to read()

Modular structure of the LLRF server

- 3 big module groups:
  - AdcBoard: direct signal monitoring
  - Controller: monitor feedback loop, generate control tables etc.
  - Automation: ramping (optional)
- Can have multiple AdcBoard groups for more channels (e.g. for multi-cavity systems)
- MicroDAQ system writes data to HDF5 file

Information model with tags

- Model incomplete, full model too big to show

Status of ApplicationCore and the LLRF server

- The ApplicationCore-based LLRF server has already been tested successfully in DOOCS environments
- Recently successful integration tests at HZIRI/ELBE: driving a cavity with full control from WinCC over OPC UA
- CPU usage seems to be like the previous plain-DOOCS server (but runs faster due to improved multi-threading)
- ApplicationCore is available on Github:
  - http://github.com/ChimeraTK/ApplicationCore
  - Complete and working example available (see code on the left side)
- Documentation (work in progress): http://chimera.github.io