Overview of Improvements for the J-PARC Linac LLRF System

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Abstract

In the J-PARC linac, the LLRF system with the digital feedback (DFB) and the digital feedforward (DDF) was adopted for the satisfaction of amplitude and phase stabilities and is was operated without serious problems. However, almost all modules of the 324MHz system have been used since the beginning of the J-PARC and are more than ten years into the development. The increase of the failure frequency for this system is expected. In addition, it is difficult to maintain it for some discontinued boards of DFB and DFF and the older OS and developing environment of software. Therefore, we are starting to study the new LLRF system of the next generation. In the present, we are exploring several possibilities of a new way and investigating each advantage and disadvantage.

Introduction

In the J-PARC linac, the energy of the injecting beam to RCS was upgraded to 400 MeV by the installation of 25 ACS modules in the shutdown of 2013 and 4080 MeV acceleration was successfully achieved on January 17th. In addition, the intensity upgrade was down to achieve the design power of 1 MW by improving the front-end on the shutdown of 2014. The LLRF system with the digital feedback (DFB) and the digital feedforward (DDF) was adopted for the satisfaction of amplitude and phase stabilities and is was operated without serious problems. However, almost all modules of the 324MHz system have been used since the beginning of the J-PARC and are more than ten years into the development. The increase of the failure frequency for this system is expected.

Therefore, we are developing a new digitizer instead of the digital boards of cPCI. In the 1st stage, a digital board with the platform of µTCA.4 will be produced. Here the RTM board will be temporary but the AMC will become a specialized board. The shelf with the bus and the RF backplane will not be used and the AMC board will be used for the Ethernet LAN connection. In the next stage, we would like to develop an analog board of a µTCA.4 RTM.

Installation of a new digitizer

Present system:

command: PLC-TP at local & PC at remote → LLRF-PLC → cPCI monitor: cPCI → LLRF-PLC → PLC-TP for local & PLC for remote

Considering system: new digitizer with EPICS-JOC, PLC ladder → only interlock command: PC → digitizer, and PC → PLC(interlock)

monitor: digitizer → PC, and PLC(interlock) → PC

Test digitizer (miner change of STF)

FMC carrier signal processing board producing Mitsubishi Electric TOKKI Systems Corporation platform: µTCA.4 AMC
FPGA: Zynq XC7Z045-1FFG900C, QSPI FLASH-ROM 16MB, SD-Card Remote Update
RAM: DDR3-3DRAM 1GB x2 (PL, PS)
OS: Xilinx Linux (EPICS-JOC)
FMC: High pin count, Low pin count
High count pin, Low pin count
ADC: 13ch 16bit 370MSPS on FMC card
DAC: 2ch 16bit 500MSPS on FMC card

On the test using a mock cavity without beam

Amplitude Stability: -0.1% (p-p)
Phase Stability: -0.1 deg (p-p)

New schedule:

Test at a 3MeV beam test accelerator facility (IS + RFQ cavity)
27 Oct.: test without beam
5 Nov.: test with beam

Digitizer prototype under consideration

A/D-D/A signal processing board producing Mitsubishi Electric TOKKI Systems Corporation platform: µTCA.4 AMC
FPGA: Zynq XC7Z045-1FFG900C, QSPI FLASH-ROM 16MB, SD-Card Remote Update
RAM: DDR3-3DRAM 1GB x2 (PL, PS)
OS: Xilinx Linux (EPICS-JOC)
ADC: 8ch 16bit 370MSPS(max.), BW: 800MHz
DAC: 2ch 16bit 500MSPS
SFP: 2ports

The µTCA.4 RTM of the J-PARC linac LLRF will be produced.

just level converter: In the 1st step, analog modules of cPCI are used.

Test stand for test digitizer.

Download the full PDF for more detailed information.