Overview of Improvements for the J-PARC Linac LLRF System

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Abstract

In the J-PARC linac, the LLRF system with the digital feedback (DFB) and the digital feedforward (DFF) was adopted for the satisfaction of amplitude and phase stabilities and is was operated without serious problems. However, almost all modules of the 324MHz system have been used since the beginning of the J-PARC and are more than ten years into the development. The increase of the failure frequency for this system is expected. In addition, it is difficult to maintain it for some discontinued boards of DFB and DFF and the older OS and developing environment of software. Therefore, we are starting to study the new LLRF system of the next generation. In the present, we are exploring several possibilities of a new way and investigating each advantage and disadvantage.

Introduction

In the J-PARC linac, the energy of the injecting beam to RCS was upgraded to 400 MeV by the installation of 25 ACS modules in the shutdown of 2013 and the 400-MeV acceleration was successfully achieved on January 17th. In addition, the intensity upgrade was down to achieve the design power of 1 MW by improving the front-end on the shutdown of 2014.

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Therefore, we are developing a new digitizer instead of the digital boards of cPCI. In the 1st stage, a digital board with the platform of μTCA.4 will be produced. Here the RTM board will be temporary but the AMC will become a specialized board. The shelf with the bus and the RF backplane will not be used and the AMC board will be used for the Ethernet LAN connection. In the next stage, we would like to develop an analog board of a μTCA.4 RTM.

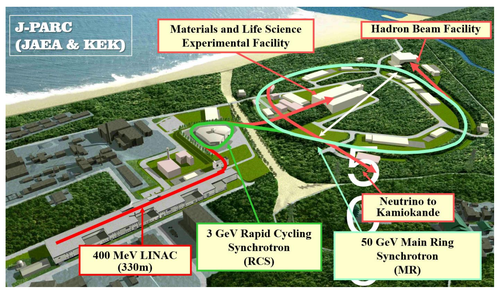

Figure 1: Overview of J-PARC

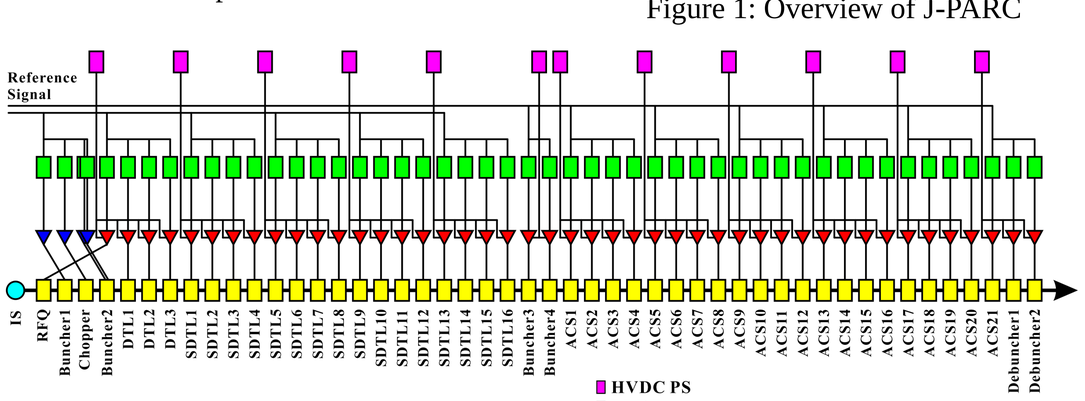

Figure 2: RF system of the J-PARC linac. There are twenty-four 324-MHz LLRF stations and twenty-five 972-MHz stations.

#Components	HVDC PS	LLRF	Klystron	Solid-State Amplifier	Cavity Module
324MHz	5	24	20	4	23
972MHz	7	25	25	0	25

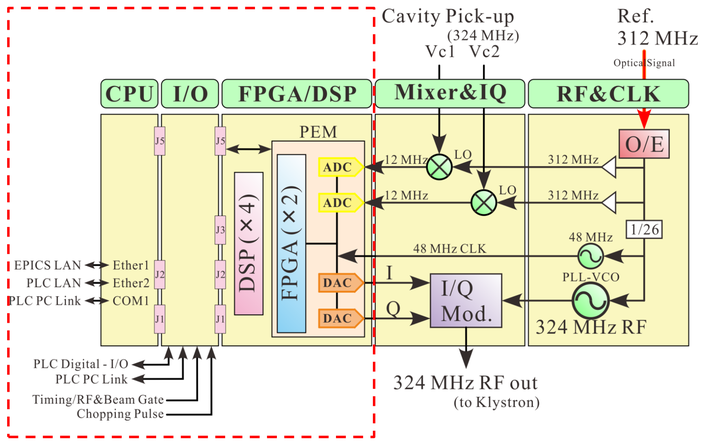

Figure 3: Digital LLRF system using the cPCI boards at the J-PARC linac. We are planning to improve the digital boards at the 1st step.

Present Status

cPCI board

- ✓ FPGA board: discontinued
- ✓ DSP board: discontinued
- ✓ CPU board: discontinued, but fungible

Development enviloment

- ✓ FPGA: Xilinx ISE Ver 6.2i
- ✓ DSP: TI Code Composer Studio Ver 2.1
- ✓ Host program: Redhat 8.0 gcc compiler Ver 3.2
- ✓ Application: wxPython 2.6

Installation of a new digitizer

Present system:

command: PLC-TP at local & PC at remote → LLRF-PLC → cPCI
monitor: cPCI → LLRF-PLC → PLC-TP for local & PLC for remote

Considering system: new digitizer with EPICS-IOC, PLC ladder → only interlock

command: PC → digitizer, and PC → PLC(interlock)
monitor: digitizer → PC, and PLC(interlock) → PC

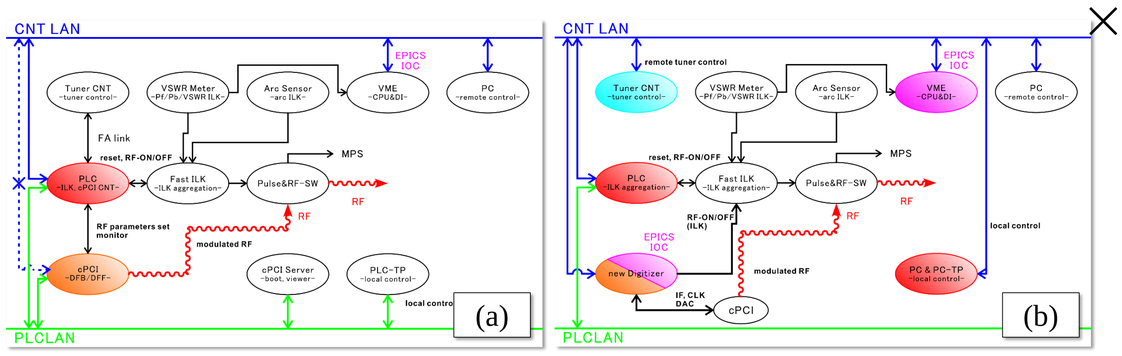

Figure 4: (a) present LLRF system and (b) new LLRF system under consideration. In the present system, all monitored signals and parameter setting commands go through LLRF-PLC. But then, a new digitizer has a capability of EPICS-IOC and some monitors and commands do not go through LLRF-PLC.

✕ *logic in the LLRF-PLC*

ladder

- auto-tuner
- auto-start_up
- auto-conditioning
- quick recovery
- …

✕ *PLC-TP for local control*

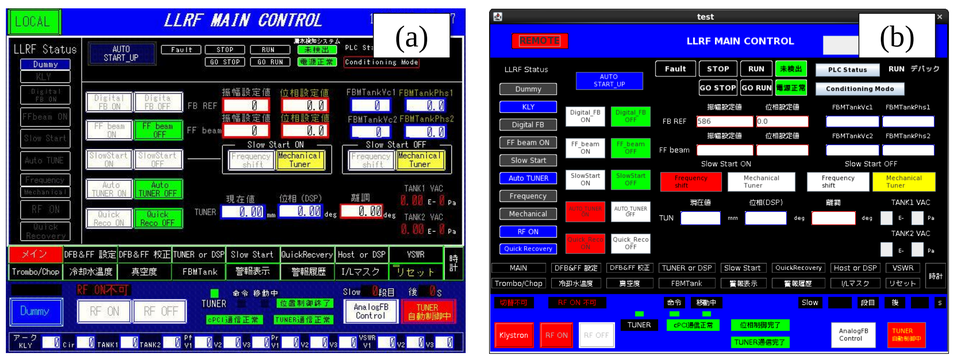

Figure 5: (a) present local control interface and (b) developed local control interface.

New system:

- ➢ auto-tuner: by EPICS record (on development)
- ➢ auto-start_up: by carbon shell script (almost done)
- ➢ auto-conditioning: by java program (almost done)
- ➢ quick recovery: by contact signal & PLC ladder
- ➢ PLC-TP: small PC + display with touch-panel operation (on development)

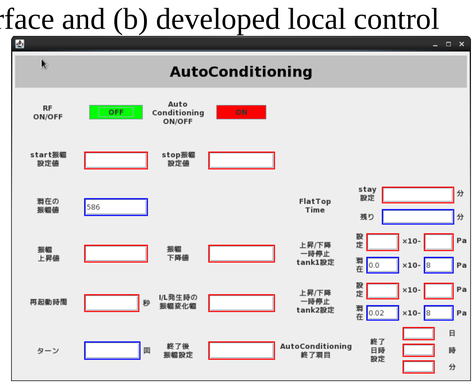

Figure 6: GUI for Auto-conditioning.

Test digitizer (miner change of STF)

FMC carrier signal processing board producing Mitsubishi Electric TOKKI Systems Corporation

platform: μTCA.4 AMC
FPGA: Zynq XC7Z045-1FFG900C,
QSPI FLASH-ROM 16MB,
SD-Card Remote Update
RAM: DDR3-SDRAM 1GB✕2 (PL, PS)
OS: Xilinx Linux (EPICS-IOC)
FMC: High pin count, Low pin count
ADC: 13ch 16bit 370MSPS on FMC card
DAC: 2ch 16bit 500MSPS on FMC card

→ minor change of STF test module

On the test using a mock cavity without beam

- Amplitude Stability: <0.1% (p-p)
- Phase Stability : <0.1 deg. (p-p)

→ one order less than requirements (amplitude: 1%, Phase: 1deg.)
→ but cannot use RF backplane in the future (CLK should be inputted from the AMC front)

New schedule:
Test at a 3MeV beam test accelerator facility (IS + RFQ cavity)

- ✓ 27 Oct.: test without beam
- ✓ 5 Nov.: test with beam

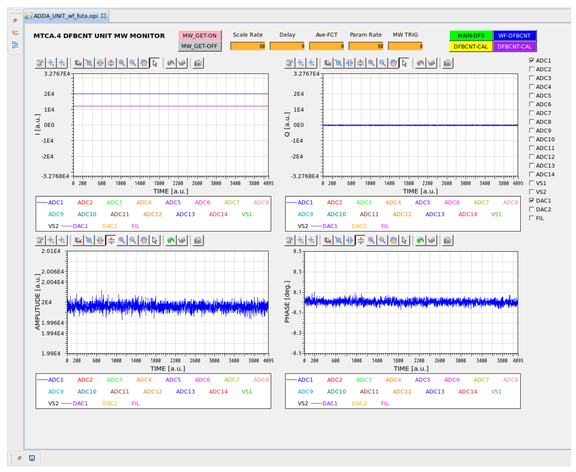

Figure 7: Stabilities of amplitude and phase using mock cavity at the test digitizer.

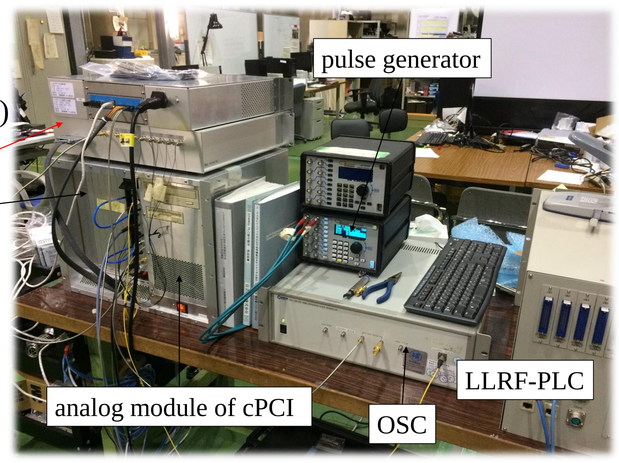

Figure 8: Test-stand for test digitizer.

Digitizer prototype under consideration

A/D-D/A signal processing board producing Mitsubishi Electric TOKKI Systems Corporation

platform: μTCA.4 AMC
FPGA: Zynq XC7Z045-1FFG900C, QSPI FLASH-ROM 16MB, SD-Card Remote Update
RAM: DDR3-SDRAM 1GB✕2 (PL, PS)
OS: Xilinx Linux (EPICS-IOC)
ADC: 8ch 16bit 370MSPS(max.), BW: 800MHz
DAC: 2ch 16bit 500MSPS
SFP: 2ports

→ The μTCA.4 RTM of the J-PARC linac LLRF will be produced.
(just level converter. In the 1st step, analog modules of cPCI are used.)

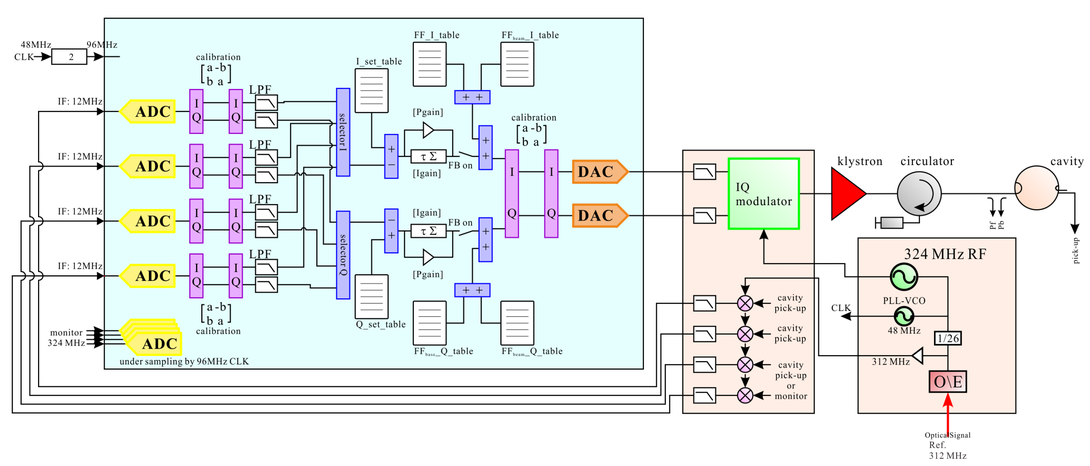

Figure 9: A new digitizer under consideration. There are four ADCs measuring IF signals and four ADCs measuring direct sampling.

ex. ADC1,2(mixer(IF:12MHz) + IQ sampling(96MHz CLK)): cavity pick-up
ADC3,4(mixer + IQ sampling): directional coupler(Pf)
ADC5(direct sampling(96MHz CLK)): input of 40W amplifier
ADC6(direct sampling): input of klystron
ADC7(direct sampling): output of klystron
ADC8(direct sampling): neighbor cavity