DIGITAL LOW LEVEL RF SYSTEMS FOR DIAMOND LIGHT SOURCE

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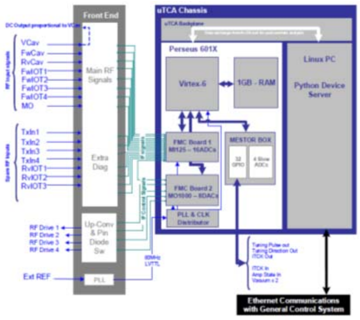
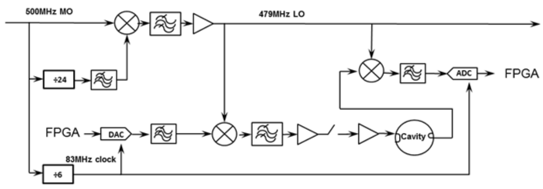
Introduction

Two new normal conducting cavities have been constructed and are being installed in the Diamond Light Source storage ring. A digital LLRF system has been developed with ALBA Synchrotron for these new cavities. The digital system will offer improved functionality in comparison to the analogue systems currently employed at Diamond, and once proven on the new cavities, will be deployed for the existing superconducting storage ring cavities and multi-cell normal conducting booster cavities. The new digital LLRF is based on Virtex6 FPGA and fast ADCs and DACs. One system has been built and verified in the Diamond booster with beam and in the Diamond RF Test Facility with the new design of normal conducting cavity. Test results and plans for the future are presented.

DLLRF Hardware

The new DLLRF was based on the MicroTCA standard. It was chosen for its reliability, modularity and scalability. A commercial advanced mezzanine card (AMC), Perseus 601X with Virtex6 FPGA from Nutaq, is used as the core processor of the control algorithm. 16 Channel 14-bit ADCs and 8 channel 16-bit DACs FPGA mezzanine cards (FMC) are used for analogue input and out interface.

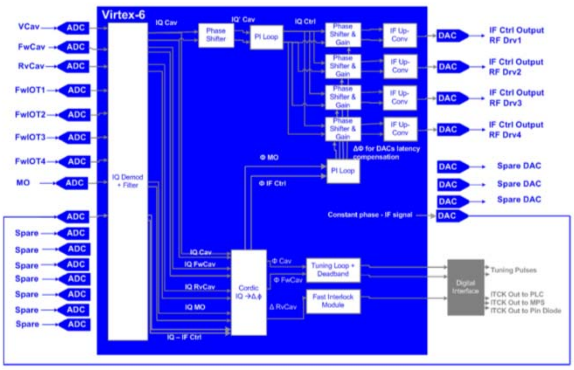




Schematic of RF signal processing.

DLLRF Firmware

- IQ or polar PI loops of the cavity field to control amplitude and phase.
- Cavity tuning.
- Fast interlocks handling.
- Automatic start-up of the system.
- Automatic conditioning of the cavity
- Monitoring of RF signals.
- Recording of main digital processing signals for post-mortem analysis.



DLLRF Performance

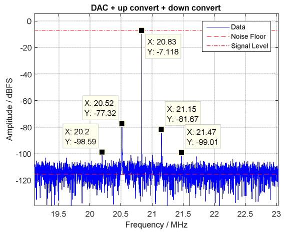
The DLLRF has been tested at low and high power, and has been used with beam in the Diamond booster, and for conditioning of two storage ring cavities in the Diamond RF Test Facility.

ADC Test

The raw data from ADCs were retrieved using the fast data logger. Performance was consistent with the specification of the ADC. A 70 dB SNR was achieved.

ADC test results

- Amplitude jitter 0.055% RMS
- Phase jitter 0.035° RMS



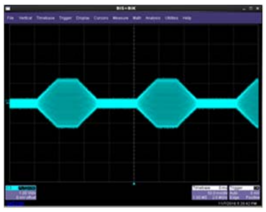
FFT of raw ADC data

High Power Test

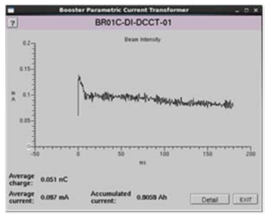
The new DLLRF was installed in the booster RF system and was connected to the high power amplifier and cavity. The system parameters were measured at high power. The group delay of the DLLRF was 2.2 µs. Rectangular and polar loops have similar band-width values when using similar proportional gain and integral gain values. 30 kHz bandwidth can be achieved setting high gain values.

Operation with Beam

After all the functionalities had been verified at high power, the DLLRF was tested with beam. An RF ramp was generated by the DLLRF and beam was successfully captured in the booster at 100 MeV and ramped to 3 GeV.



Ramping RF cavity field.



Captured and accelerated beam in the booster

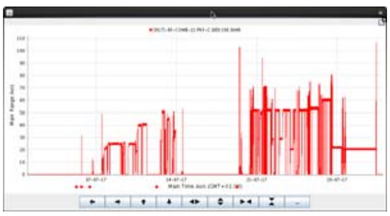
Cavity conditioning

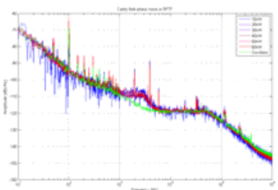
Two HOM damped cavities of the BESSY design are being installed in the Diamond storage ring. They will be controlled by the new DLLRF and have been conditioned to high power using this system

The first cavity was conditioned up to 60kW CW in July 2017 and was installed in the storage ring in August.

Plots below show the increase in forward power during conditioning and phase noise measured at the pickup at different power levels.

Conditioning of the second cavity is ongoing.





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