

HIAF (High Intensity Heavy-ion Accelerator Facility) Synchrotron LLRF R&D

Yan Cong, Zhe Xu, Ruifeng Zhang, Shilong Li, Xiaodong Han Institute of Modern Physics, Chinese Academy of Sciences

## Introduction Cavity Structure Hardware

According to the task of the HIAF (High intensity Heavy-ion Accelerator Facility) synchrotron project undertaken by the Institute of Modern Physics, Chinese Academy of Sciences, we need to develop a RF system of a MA core loaded cavity. The RF system is mainly consists of four parts: MA loaded cavity, high power pulse power source, full digital LLRF and computer control system. Table 1 is the specification of the RF system of the MA loaded cavity, figure 1 shown the accelerating voltage, synchronous phase and RF frequency with time of the four operating mode.

MA loaded cavity has the advantages of high impedance, wide band, fast response speed, high acceleration gradient. the cavity plan to use Febased nano magnetic alloy core as loading material.



LLRF board is a signal processing board, which is designed base on Xilinx V5 series chip.



Specification of RF system of the MA loaded cavity

Working frequency	0.29~0.98 MHz
Repetition frequency	0.33 Hz
Duty cycle	50%
Working mode	Sweep frequency
	mode
Peak voltage	40kV
Minimum voltage	1kV
Voltage rise time	10µs
Phase stability,	≤ <b> 1</b> °
Amplitude stability	≤ 1×10 <sup>-2</sup>





**Multi-Control Loops** 



Figure.6 LLRF Board Topology



Figure.7 ADC/DAC Board Topology



2) Beam loading compensation. Use Feed-forward to cancel the beam loading effect.
3) Synchronous phase control loop. Damp the longitudinal dipole oscillation.

## BPM FCT Gavity

Figure.3 Reference Principle Diagram of the Multi-Control Loops

## **Beam Loading**

Two methods will be used to compensate the beam loading, one is analog direct feed back, the other is feed forward.





Figure.8 LLRF Board

## Challenge

Beam loading compensation
 It's a new thing for us. We should carefully
 calculate the change of cavity impedance
 caused by beam current.

4) Radial feed-back loop. Adjust the working frequency according to BPM signal.

5) Load amplitude, synchronous phase and working frequency set value from data file.6) All digital system.

7) Hardware base on cPCI bus.

8) EPICS interface.

Figure.4 Schematic Diagram of Direct Feed-back Transmitter



2) low operating frequency

range.

In order to obtain the zero IF signal after quadrature demodulation, we need to reduce the sampling rate. But this will reduce the system's response speed.

3) Big dynamic range of cavity impedance The parallel impedance of cavity will change from  $330 \sim 450 \Omega/\text{gap}$  with frequency from  $0.29 \sim 0.98$ MHz. The amplitude stabilization loop requires a large dynamic

Figure.5 Schematic Diagram of Direct Feed-back Transmitter

