Science & Technology Facilities Council
ISIS

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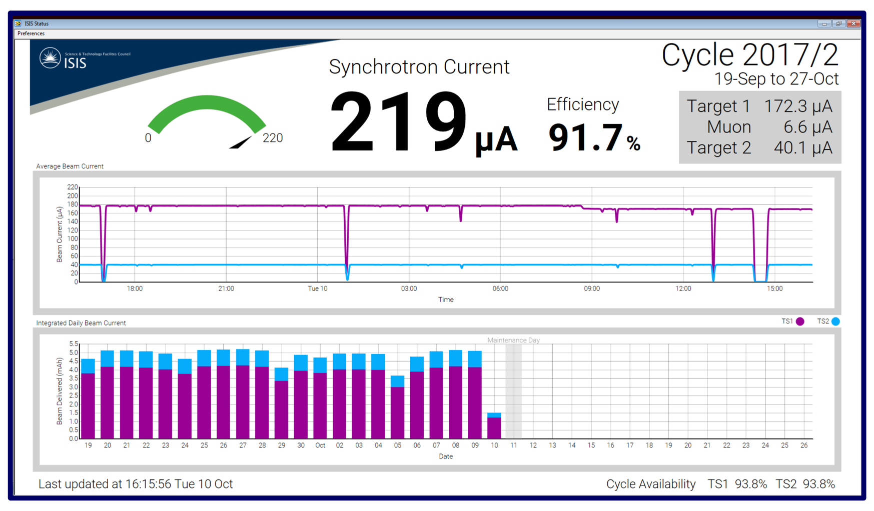
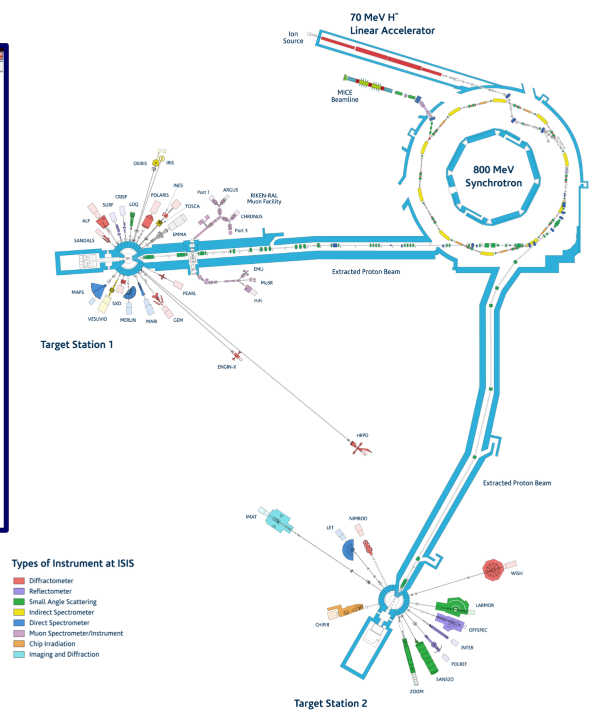
PROGRESS ON THE ISIS SYNCHROTRON DIGITAL LOW LEVEL RF SYSTEM UPGRADE

Abstract

The ISIS synchrotron at the Rutherford Appleton Laboratory in the UK now routinely uses a dual harmonic RF system to accelerate beam currents in excess of 230 uA to run two target stations simultaneously. The acceleration in the ISIS synchrotron is provided by six fundamental frequency (1RF) and four second harmonic (2RF) RF cavities. The 1RF systems are required to sweep from 1.3MHz to 3.1MHz during the 10ms acceleration period, repeated at 50Hz, with the 2RF systems sweeping from 2.6MHz to 6.3MHz. The existing analogue LLRF control system has been in service for over 30 years and is now showing some signs of old age and spare parts are becoming difficult to source.

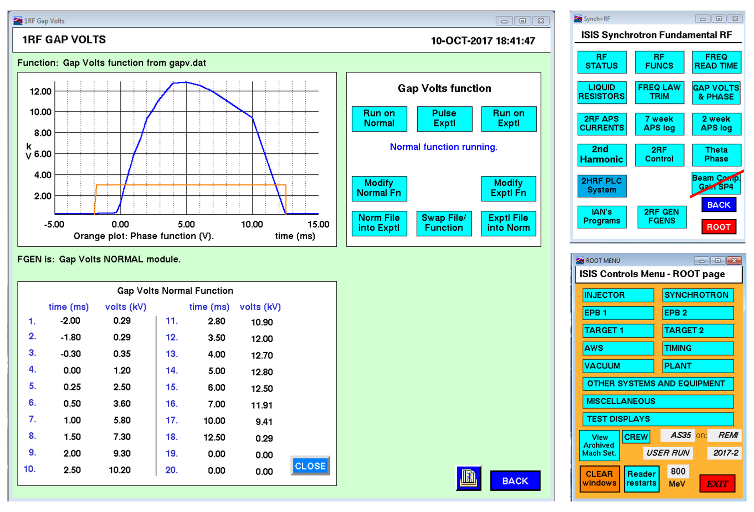




In order to overcome this and to give more stable control of the phase of the RF voltage at each of the cavities, changes have been made to the LLRF control systems. A new FPGA based combined frequency law generator / master oscillator has been implemented using “off-the-shelf” National Instruments PXI-express based FlexRIO modules. This approach has allowed the relatively rapid deployment and testing of various components of the LPRF system each with different functionality. The system has been successfully used during the ISIS operational cycles over the last eighteen months or so. This poster reports on the commissioning of the FlexRIO system and plans for the gradual replacement of remaining parts of the LPRF system.

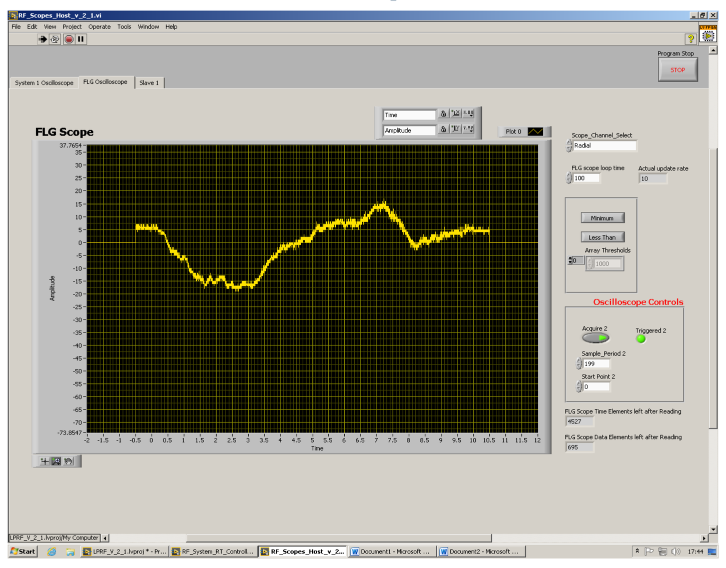
System Architecture

ISIS VISTA Controls system

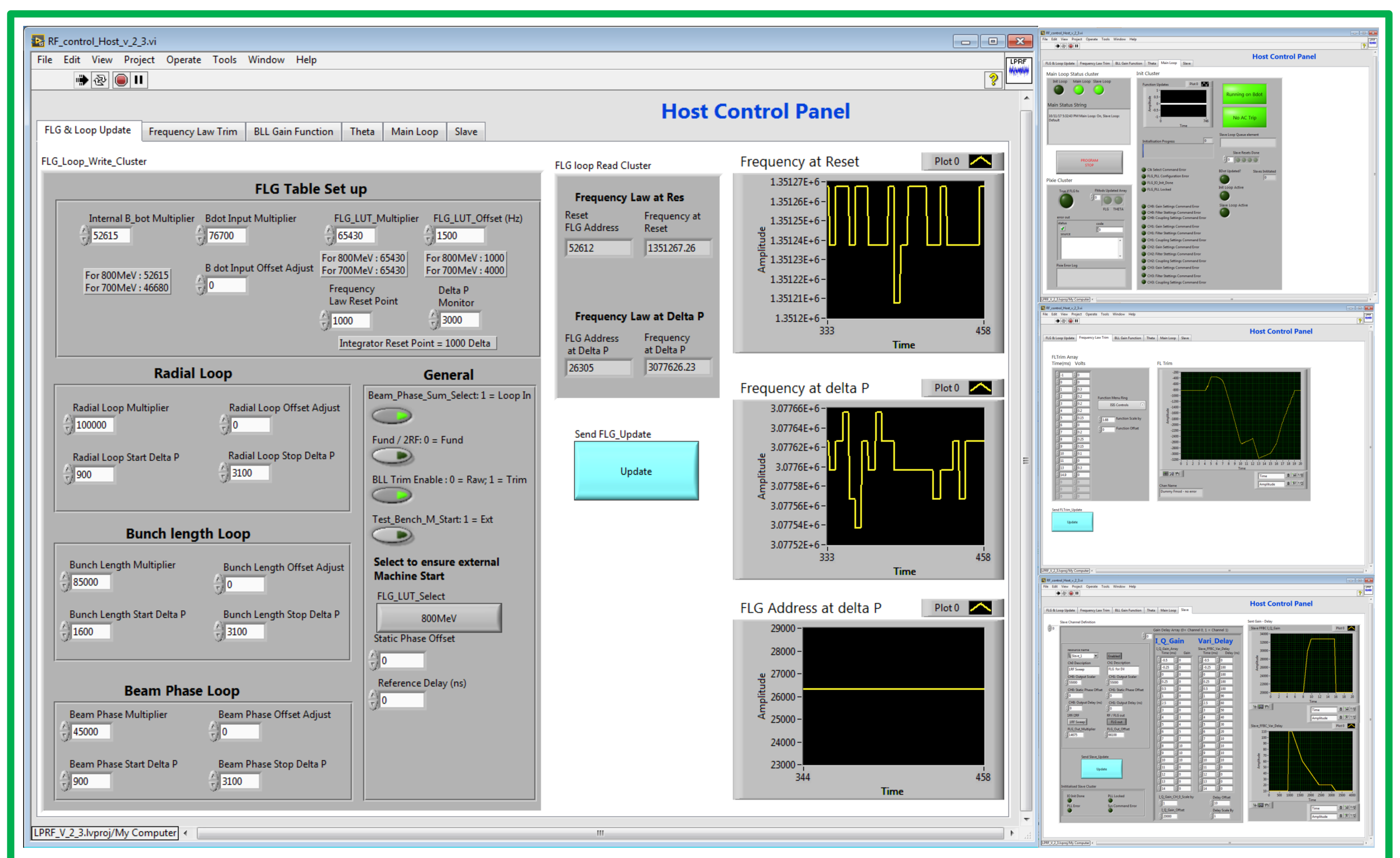


ISIS Main Controls parameters set by machine physicists / crew

Windows PC diagnostics VI (Virtual scope traces)



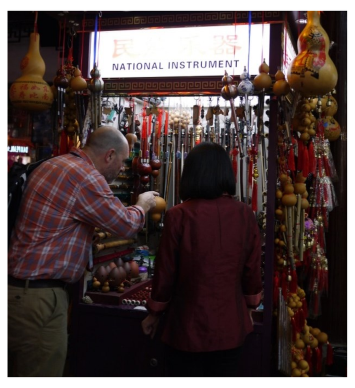
Enables selection and display of test signals and Displays. Currently available for a limited selection of virtual test points in the FPGA code eg radial loop input (shown above). Deployed on the Windows PC in the LabView development environment, with refresh rates available up to 20Hz or so, but will be rolled out as an executable.

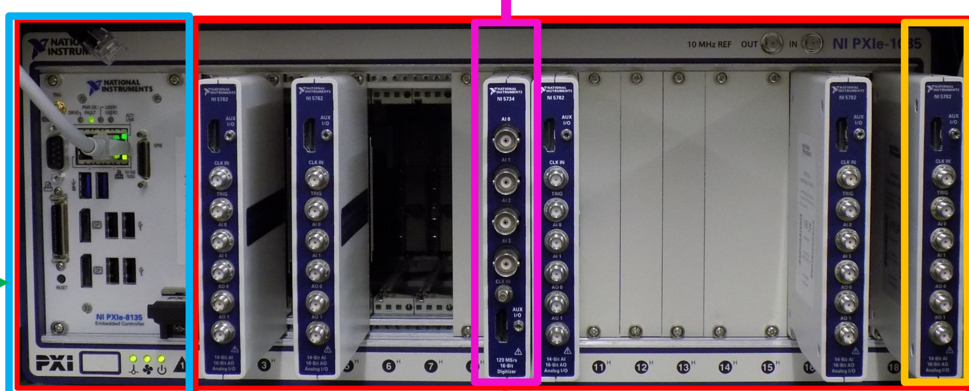


Windows PC control VI

RF setup parameters- phase offsets, Loop gains etc (set by RF team)

Web based access





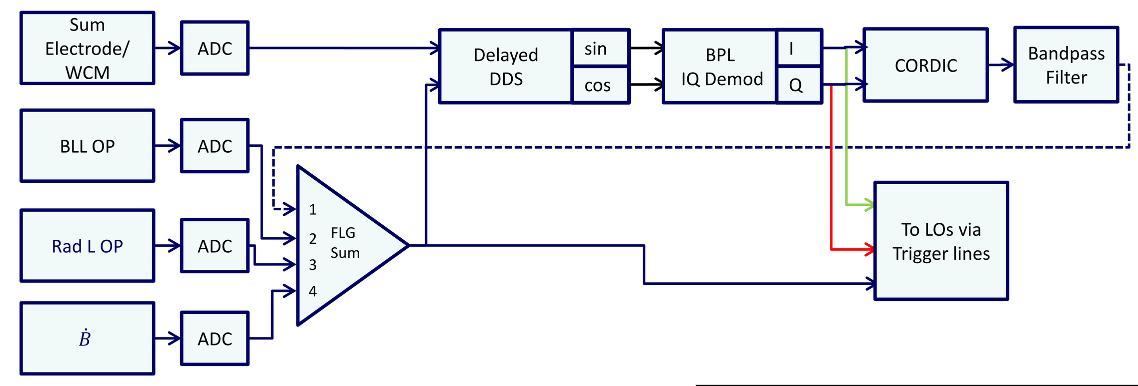
RT – OS Controller

System Timing, Freq. Increment & FF Beam Compensation broadcast over trigger lines

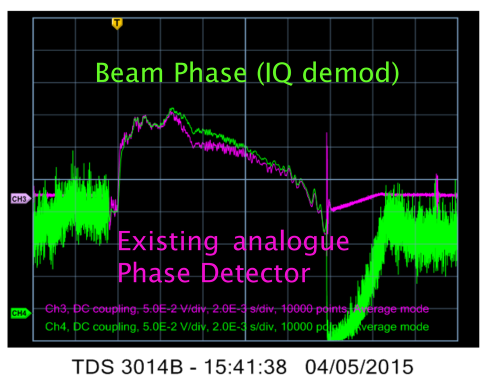
Diagnostic virtual “scope traces” sent from FPGAs to RTOS controller via 4-Lane PCIe / Switch Fabric Backplane

Frequency Law Generator / Master Oscillator

Implemented using LabView FPGA on NI PXIe7966R FPGA module + NI 5734 120MS/s digitiser adapter module generates the RF sweep from 1.3MHz to 3.1MHz for 1RF caivites and 2.6 to 6.3MHz for 2nd Harmonic cavities.

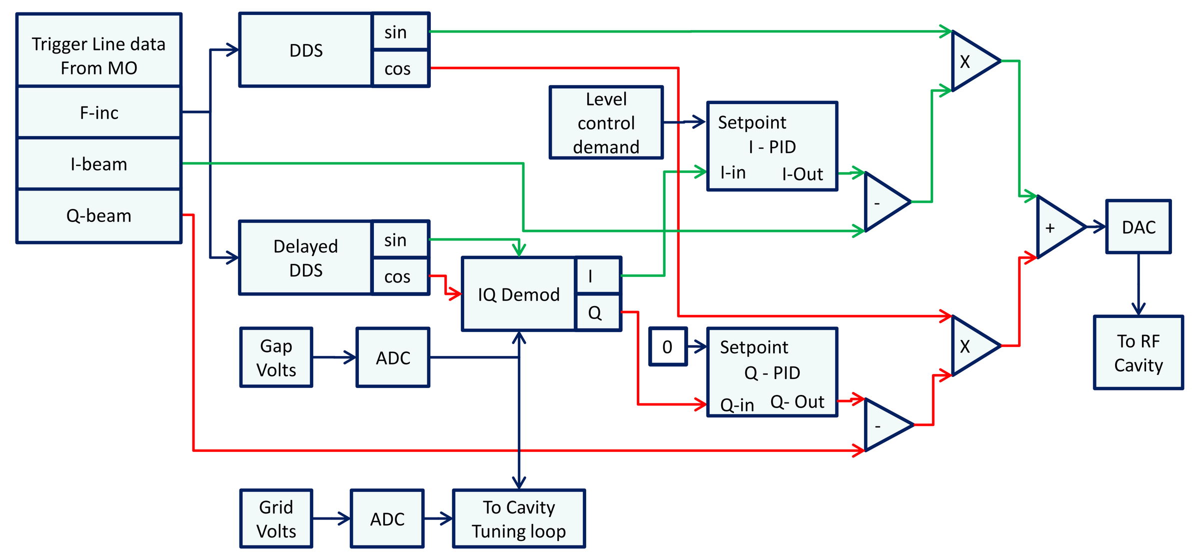


Previous tests used IQ demodulation of the beam sum electrode signal followed by a CORDIC algorithm to generate a beam phase signal. This will be implemented to replace the existing analogue beam phase loop with the added benefit of using the same beam signal to generate the Bunch Length Loop correction.



Local Oscillator

Implemented using LabView FPGA on NI PXIe7966R FPGA module (Virtex-5 SX95T FPGA /512 MB DRAM) + NI5782 250MS/s IF transceiver adapter module (6 x 1RF modules + 4 x 2RF Modules)



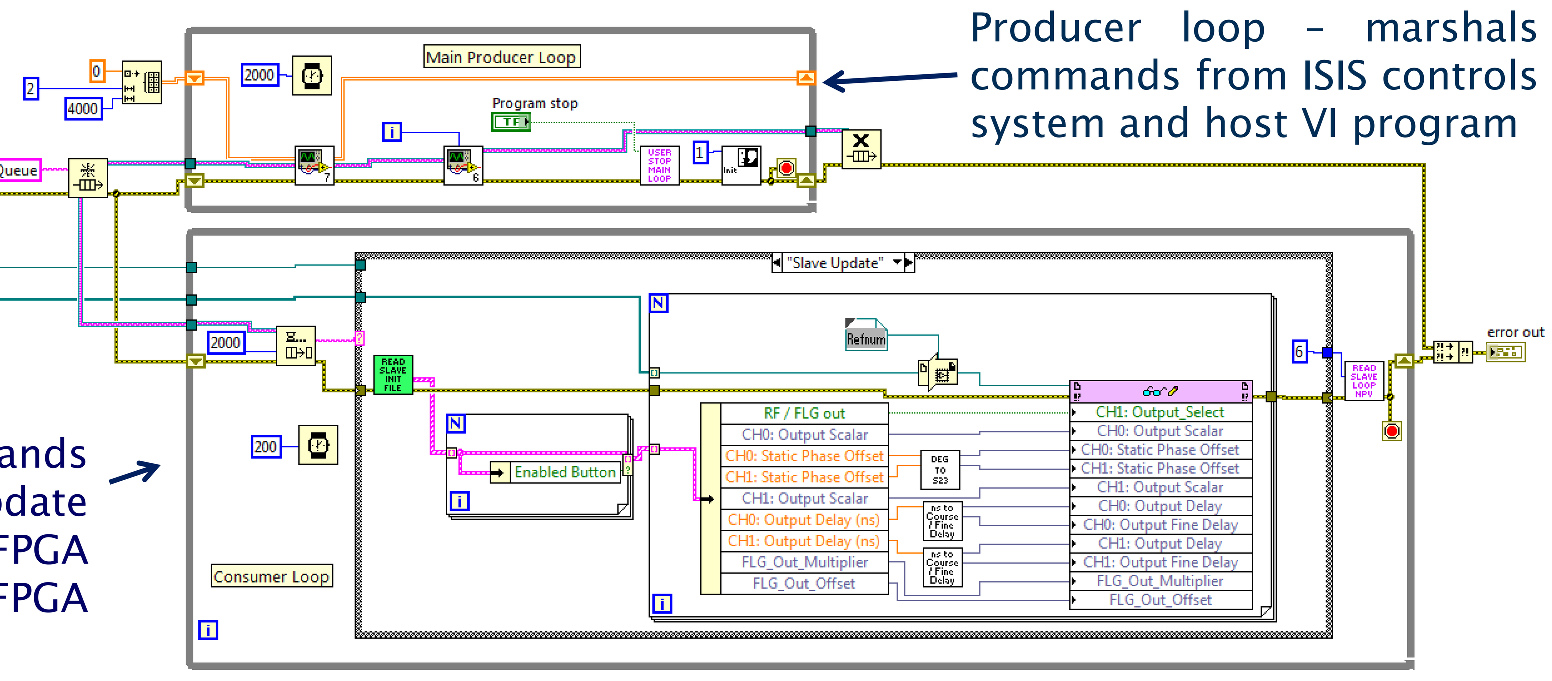
LO PID control loops

- Amplitude & Phase control on cavity using PID control loops for both I & Q vectors (10KHz Loop Response required)
- Will extend to Cavity tuning loop in the future (and have investigated use of reference signal to replace grid volts)

NI Realtime Controller

Boot-up executable file that downloads the bitfiles to each FPGA on power up, performs initialisation and clock synchronisation of the FPGA Modules.

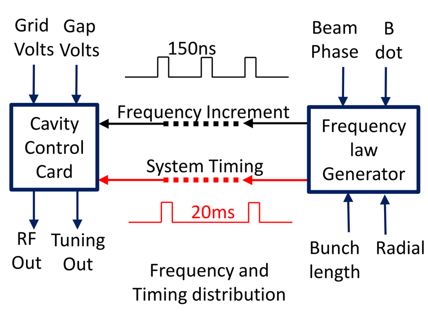
Consumer loop – selects commands from producer loop to update parameters on Master Oscillator FPGA and each of the Local Oscillator FPGA Modules..



Producer loop – marshals commands from ISIS controls system and host VI program

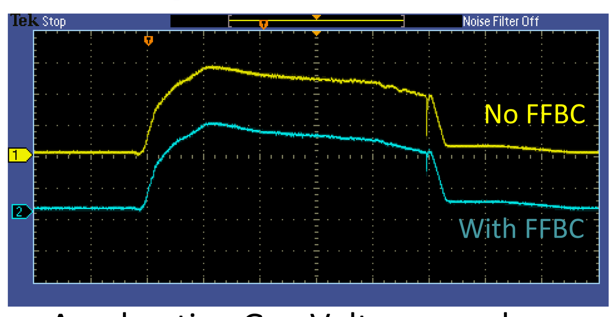
RF Synchronisation

Backplane trigger/data lines used for system timing, frequency increment broadcast and synchronous update, and beam I/Q components for feed forward beam compensation



IQ-based Feed Forward Beam Compensation

We have investigated using IQ demodulation of the beam sum signal to generate a feed-forward correction to compensate for beam loading of the RF cavity.



Accelerating Gap Voltage envelope

This has been implemented in the analogue system to replace existing filtered and delayed beam signal as this method can be easily used throughout the 2.6-6.3MHz frequency sweep of the 2nd harmonic RF cavities. Applying this technique over the last 3ms of the acceleration cycle has successfully damped down both the induced gap voltage error and the beam oscillations.

Current Status

Much of the last year has been spent solving the problem of achieving consistent synchronisation of all cavity control modules during initialisation. This has now been overcome by moving to an .exe version of the RT control software, which will be more operationally robust. This involved a re-design of the software architecture to include access of the RF parameters on the controller from the host PC. The new design will be deployed for the next ISIS user cycle in November. Initial implementation of the LO IQ control PID loop has been investigated and will be tested on the RF cavity in the coming months.

Future Development

Work on the Webserver based access to the ISIS Controls system will continue in January 2018. The limited number of control functions used in the application will be updated to include ISIS timing control and give the possibility to pulse experimental settings at lower rep rates. These will then provide a template as the digital system expands to take over more of the functionality of the existing system. The IQ demodulation scheme used in the cavity voltage control loop will be reused in the cavity tuning loop (with the further possibility of replacing the grid voltage input with a delayed reference signal to reduce instability that arises when the beam loading is providing most of the required voltage at the cavity) and also in the beam phase loop algorithm and to implement FFBC. The same beam signal will be used in the Bunch Length Loop.