A MTCA.4 BASED DIGITAL LLRF SYSTEM FOR THE GSI UNILAC

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GSI Universal Linear Accelerator UNILAC

The heavy ion linear accelerator UNILAC served for over 40 years as workhorse for nuclear physics experiments at GSI and as injector to the SIS18 synchrotron. Within the scope of the FAIR project it will also act as injector with increased requirements in beam current and beam quality. To meet these requirements and to ensure reliability for the future, a new digital low level RF system is under development. The spectrum of accelerated ions from hydrogen to uranium results in a huge dynamic range in amplitude, duty cycle and beamloading, especially in respect of the 50 Hz mixed mode. To account for the individual demands of the accelerator and to combine these with the advantages of a commercial off-the-shelf system like longterm availability and state-of-the-art technology, the new LLRF system will be based on the modular MicroTCA.4 standard.

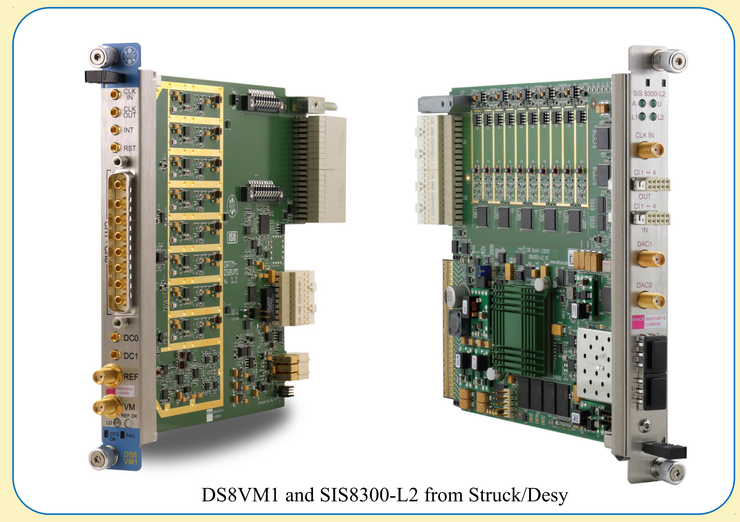
MTCA.4 Hardware

Test system 1: SIS8300-L2 & DS8VM1

- 8 AC- & 2 DC ADC channels, 16 bit, 125MHz
- 1 VM, 2 DAC channels, 16 bit, 250MHz
- Xilinx Virtex 6
- Analog circuitry (attenuator, filter, amplifier, clock generation)
- Microcontroller (MMC) for monitoring and maintenance

Test system 2: SIS8300-KU & DS8VM1

- Kintex UltraScale
- White Rabbit support



DS8VM1 and SIS8300-L2 from Struck/Desy

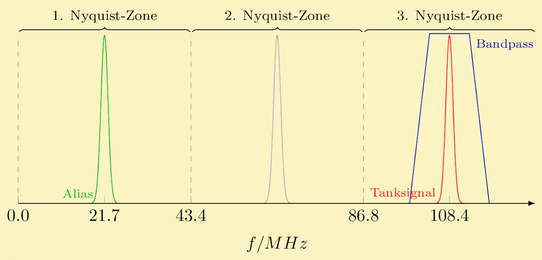
Peripheral equipment

- NAT-MCH-PHYS (MCH)
- AM 902 (CPU & SSD, Ubuntu)
- NAT-PM-AC600D (power supply)

Requirements and Features

Requirements:

- High dynamic range in pulse width (100 us ... 6 ms) and pulse amplitude (A/q = 1.0 ... 8.5)
- Various frequencies (36.1 MHz, 108.4 MHz, 216.8 MHz)
- Various transient behaviours (RFQ, IH-DTL, Alvarez)
- Non-linear amplifier characteristics (solid state, tube)
- Long-term reliability



Design:

- Direct sampling of RF signals
- Separate “slow” feedback for amplitude & phase, not controlling in I/Q space
- “Fast” adaptive and/or beam-based feedforward
- Pulse-by-pulse variable attenuators to adjust the effective range of ADC's
- Linearisation of amplier characteristics with lookup table

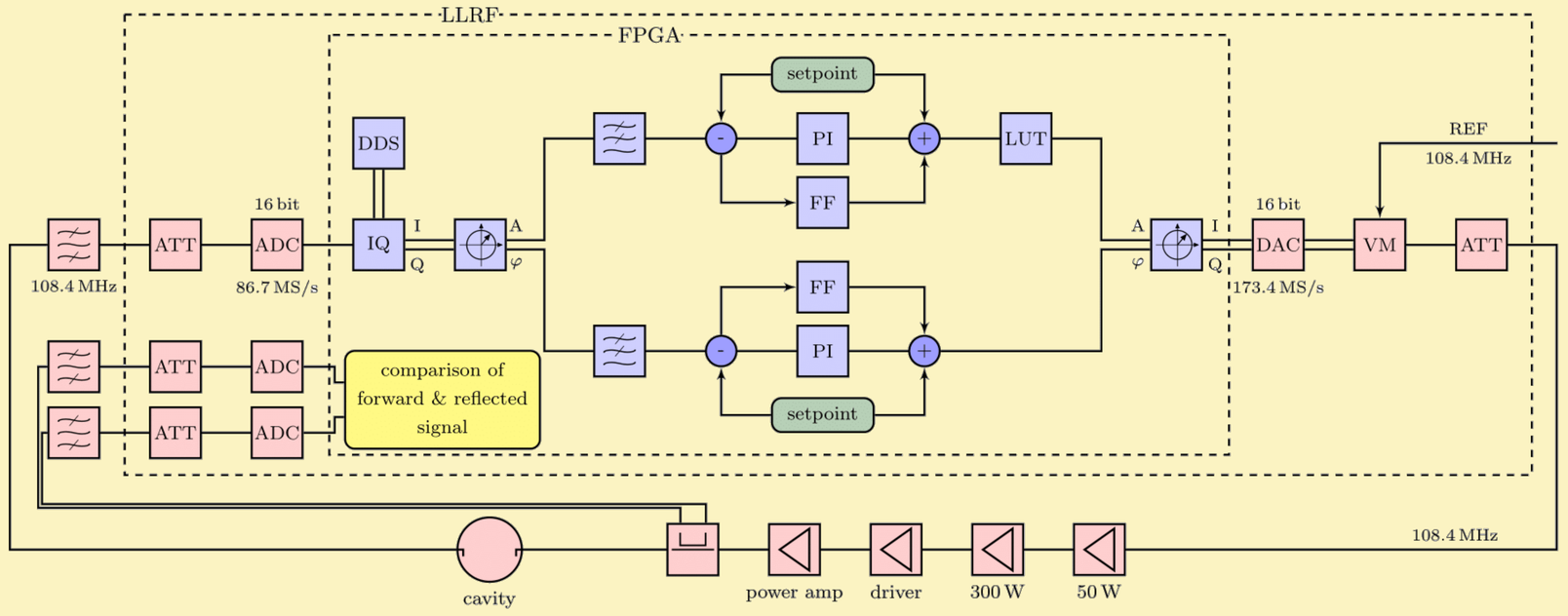
Optional Features:

- “RF tuning”: varying the RF frequency for faster warm-up process
- Network analyser functionality
- Controll the stepper motors and replace analog phase discriminator

Interface:

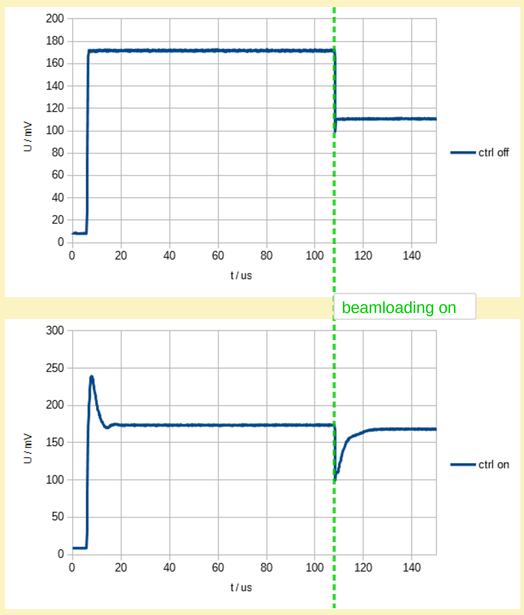
- Link to existing UNILAC analog “real-time” interface:
  - Adapter PCB using I2C over the LVDS I/O of AMC
  - 48 dig. Inputs, 16 dig. Outputs, 2 timing inputs
  - Hardware interlock for DS8VM1
- Capable to use FAIR standards FESA and WhiteRabbit in the future:
  - Data: FPGA connected to CPU via PCIe x4 Gen2
  - Timing: WhiteRabbit receiver AMC
- Local expert GUI: QT based

Block diagram



REF signal is also used to generate ADC, DAC and FPGA clock signal

First tests



First RF tests with beamload-simulation demonstrate the need for a “fast” feedforward, although there is potential to significantly reduce dead time in the control firmware.

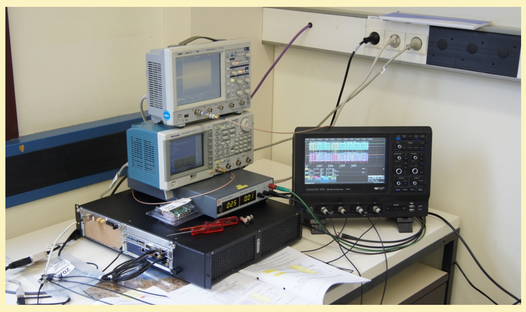
TL;DR

Current status

- UNILAC interface adapter developed and tested
- First RF tests without cavity conducted
- Stepper motor controller adapted for serial interface

Outlook

- Refining control loop
- Feedforward realisation
- Develope expert GUI for setup and monitoring
- Create FESA class



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