Beam Synchronous Processing: Fixed Clock and RF Regeneration. New Paradigms for CERN SPS LLRF

LLRF 2017

UNIVERSITAT POLITÈCNICA DE CATALUNYA BARCELONATECH

CERN

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UPGRADES & NEW PROJECTS

Higher Beam Current

Beam Synch. Processing

One Turn Feedback

Beam loading

Cavity impedance

Distance or Time of flight

Clock Synchronization RF Distribution

High Tech SoC

Deterministic Networks

Standards uTCA

IMPLICATION OF NEW ALGORITHMS ? NEW TECHNOLOGIES ?

SPS Upgrade
LIU Project

Machine Scaling

FCC hh ee he

ARE NEW TECHNOLOGIES FOR US?

PROMISING RF DISTRIBUTION AND SYNCHRO.

CONTEXT

-MOTIVATION

-BACKGROUND

-OBJECTIVE

-SOLUTIONS

-WRAP UP

-YOUR TIME…

- Classic distribution of RF
- Clock recovery from the RF

→

- Local Regeneration of RF
- Use of Deterministic Link for FTW and phase distribution
- Clock extraction from data stream of deterministic link

RECALL: RF OF CERN SYNCHROTRON'S IS RAMPED

(energy increase)

- Sweeping clock for electronics
- Custom and NIM / VME modules

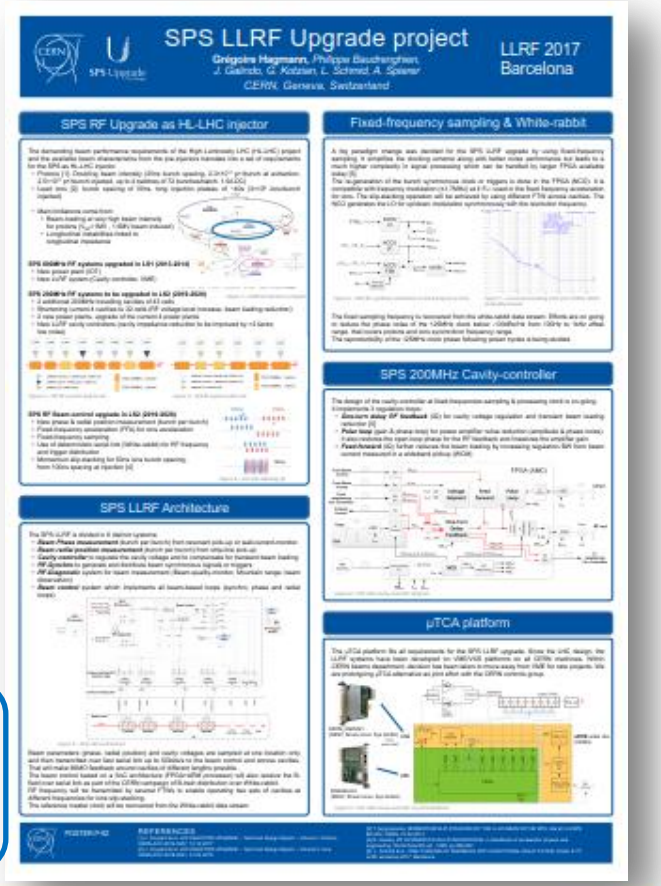
→

- Fixed clock
- uTCA

BEAM SYNCHRONOUS PROCESSING WITH FIX CLOCK

DEMONSTRATOR: ONE TURN FEEDBACK ALGORITHM

SPS 200 MHZ LLRF CAVITY CONTROLLER



DISTRIBUTED ARCHITECTURE

	Clock extracted from RF	Dedicated clock distribution
CLOCK INTERRUPTION BETWEEN CYCLES	Periodic resynchronizations require RF interruptions, which induces clock interruption in electronics	Dedicated clock can independently handle RF generation and DSP processing
SPECTRAL PURITY OF THE CLOCK	Beam Phase Loop continuously modulates RF on top of sweep Cleaning PLL architectures at specific frequencies Spectral purity of reconstructed clock not optimal Beam parameters relying on the RF noise	Dedicated cleaning architecture for clock Optimal spectral purity Optimal beam parameters
RF GYMNASTICS	Manipulations of the RF parameters. Slip stacking merging bunches in the phase space will not be possible. Fast or abrupt modifications of the phase or frequency of the RF complicated as it affects the ADC-DAC-FPGA clocking	Dedicated clock for DDS enables Digital RF regeneration Instantaneous modifications of RF phase and frequency driven by data, not by clocks Any type of RF gymnastics

FIXED CLOCK

	Swept Clock	Fixed Clock
STABILITY OF THE FEEDBACK LOOPS	Variable sampling clock → Variable loop delay Compromise in Regulation Bandwidth and Feedback Stability	Fixed sampling clock → Fixed loop delay Optimal Regulation Bandwidth and Feedback Stability
PHASE JUMPS	RF as harmonic of clock → multiplexing required to cover wide RF range Phase Jumps when multiplexing	Simple DDS implementation can cover a wider range without interruption
ADC AND DAC	Complex analogue reconstruction filter Coherent signals fall in swept range Non optimal integrated noise	Fixed analogue reconstruction filters Coherent signals at fixed digital frequencies Optimized integrated noise
UP AND DOWN MIXING	Lower spectral purity of clock → DDS and IQ sensitive to jitter → Problem for heterodyne architectures	Non IQ sampling and Direct down conversion easier
TECHNOLOGY LIMITATIONS	PLLs tracking and locking Max dF/dt for DCM in FPGAs Clock domain synchronization Complex PAR constraints Serial interfaces FIFOs	PLLs and DCM readily usable Easy place and route Ease clock domain synchronization Ease use of serial interfaces and modern technologies

WHAT IS BEAM LOADING?

Interaction between beam and accelerating cavity

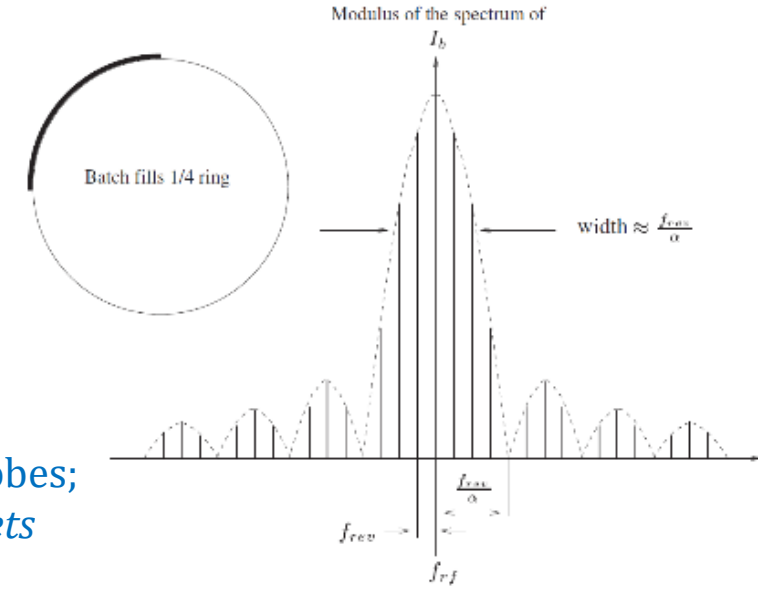
Beam induces an EM field perturbing desired cavity one

Effective accelerating voltage;

vector sum of RF generator voltage and the beam-self-induced voltage

Stationary; f_{RF}

Transient; $f_{RF} + nf_{rev}$



Revolution frequency lobes;
Irregular filling of buckets

Single line at RF frequency;
Bunch spacing multiple of the RF period, assuming that the bunch frequency is much larger than bandwidth of cavity

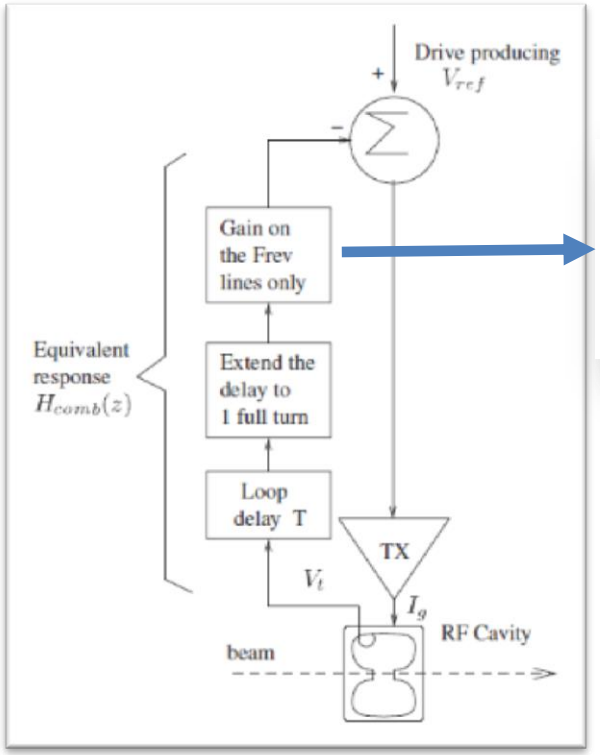
AND THE ONE TURN FEEDBACK?

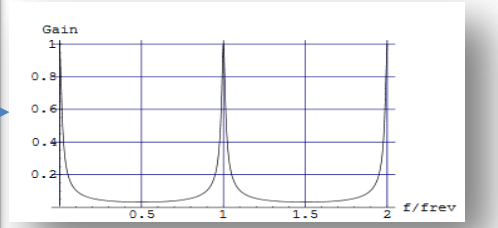
OTFB algorithm is a very old innovation at CERN, SPS Implementation

- -CONTEXT
- -MOTIVATION
- ***BACK GROUND***
- -OBJECTIVE
- -SOLUTIONS
- -WRAP UP
- -YOUR TIME…

TRANSIENT BEAM LOADING

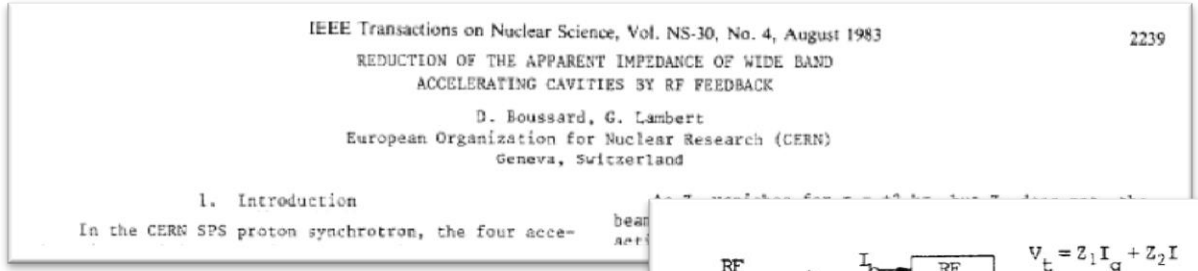
$f_{RF} + k f_{rev}$





$$H(z) = \frac{1}{1 - az^{-N}}$$

WIDE BAND
BEAM SYNC. PROCESSING


IEEE Transactions on Nuclear Science, Vol. NS-30, No. 4, August 1983 2239

REDUCTION OF THE APPARENT IMPEDANCE OF WIDE BAND ACCELERATING CAVITIES BY RF FEEDBACK

D. Boussard, G. Lambert
European Organization for Nuclear Research (CERN)
Geneva, Switzerland

1. Introduction

In the CERN SPS proton synchrotron, the four acce-

Reduction Of The Apparent Impedance Of Wide Band Accelerating Cavities By RF Feedback, BOUSSARD 1983

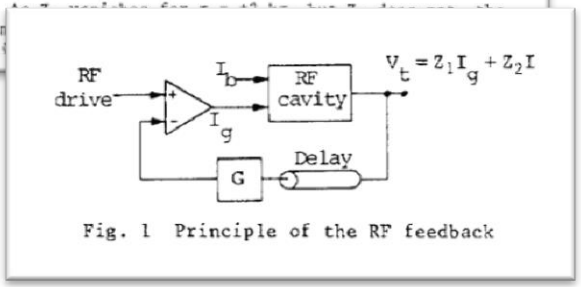


Fig. 1 Principle of the RF feedback

TODAY'S IMPLEMENTATION

***Patches** to the original design*

Custom digital module
Discrete components…

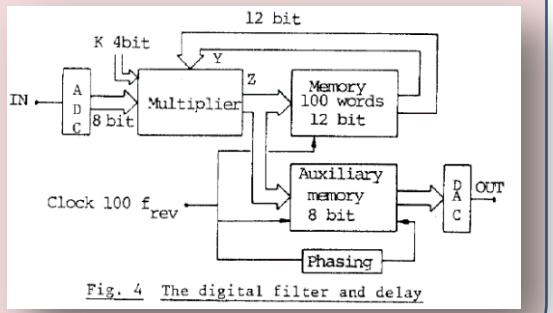


Fig. 4 The digital filter and delay

DO WE MISS SOMETHING?

SWEPT CLOCK…

WHAT DOES IT MEAN?

CLASSIC DSP SYSTEM

Sampling frequency of

ADCs, DACs, FPGAs, DSPs

is FIXED

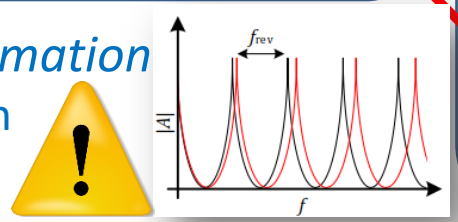
DEALING W. HARMONICS

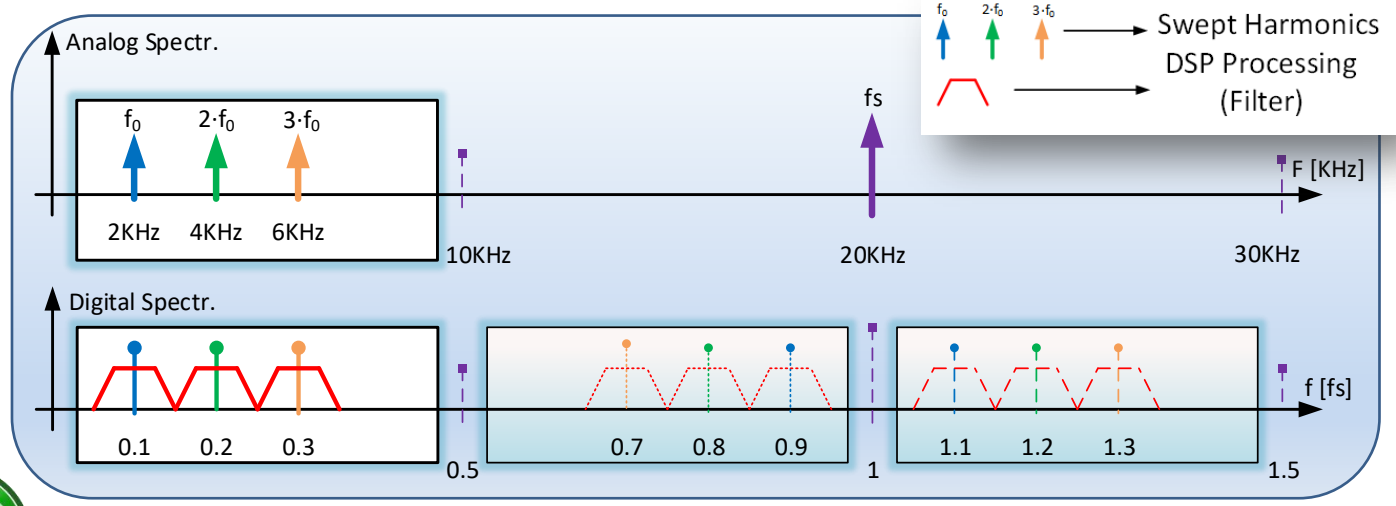
Beam Synch. Processing

Reconfig. of filters (DSP)

Homothic transformation

- harmonic position
- harmonic spacing

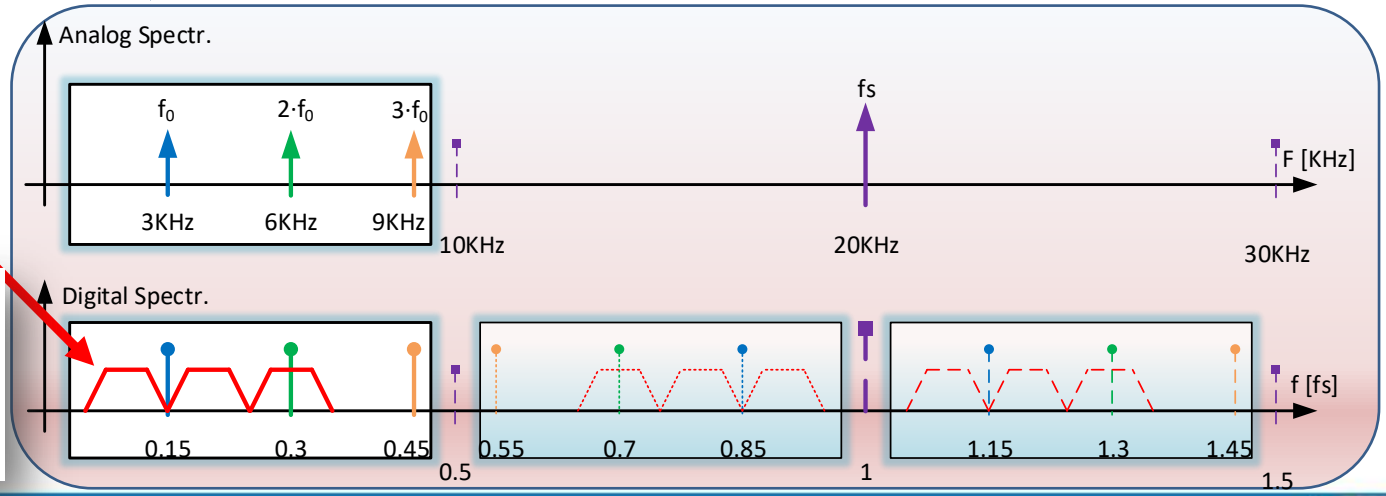




f_0: from 2KHz to 3KHz

f_s: fixed at 20KHz

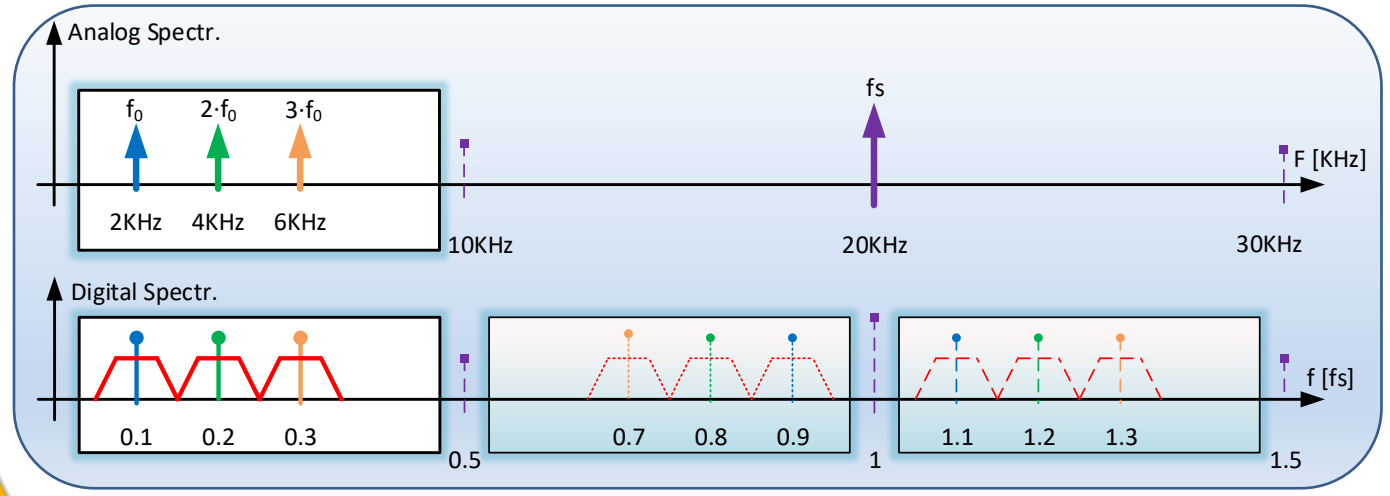
ENERGY RAMPING…
FREV MOVING



DO WE MISS SOMETHING?

SWEPT CLOCK…
WHAT DOES IT MEAN?

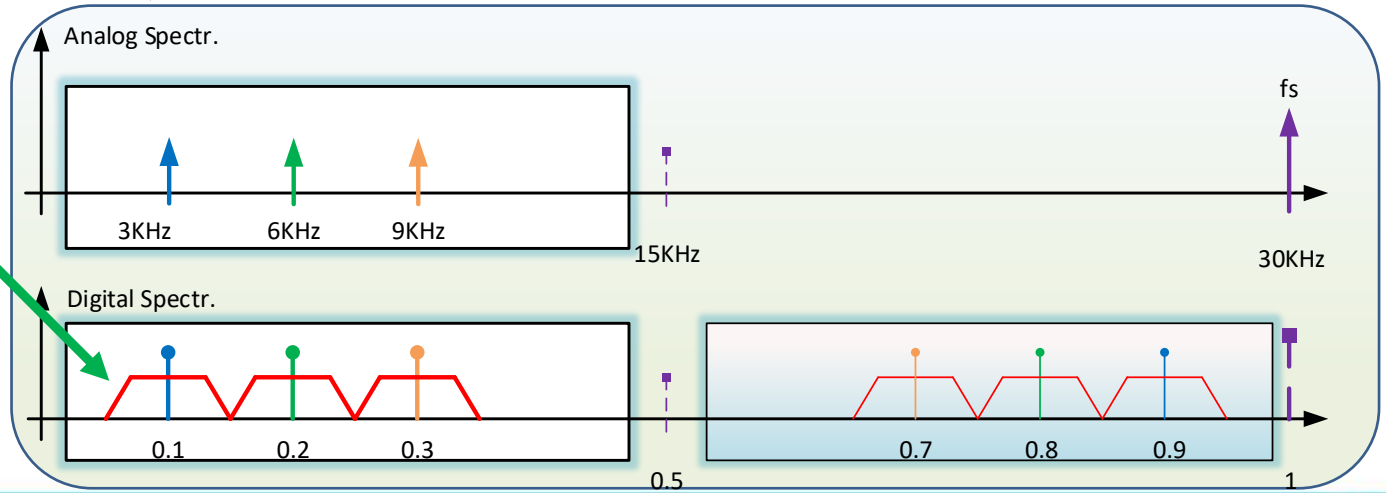
CERN DSP SYSTEM
Sampling frequency of
ADCs, DACs, FPGAs, DSPs
is SWEPT with RF



f_0: *from 2KHz to 3KHz*
f_s: from 20KHz to 30KHz

ENERGY RAMPING…
FREV MOVING

AUTOMATIC HOMOTHESIS
Filter (DSP) tracks harmonics
Beam synch. processing
One Turn Feedback algorithm



CHRISTMAS PRESENT FOR THIS YEAR…

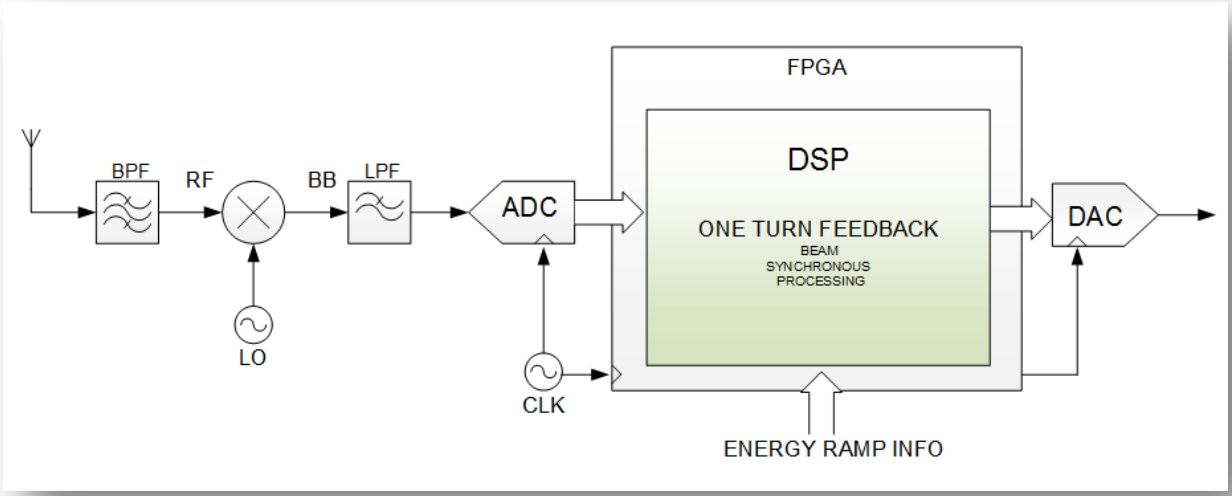
- -CONTEXT
- -MOTIVATION
- -BACKGROUND
- ***OBJECTIVE***
- -SOLUTIONS
- -WRAP UP
- -YOUR TIME…

MAY WE HAVE A ***PROBLEM*** WITH FIXED CLOCKS FOR BEAM SYNCHRONOUS PROCESSING?

OTFB Requires Homothetic Transformation

MAYBE A NEW FEEDBACK (COMB) FILTERING ARCHITECTURE???

NEW FIX CLOCK ARCHITECTURE FOR ONE TURN FEEDBACK ALGORITHM



SPECIFICATION OF THE FILTER

AIM: REVOLUTION FREQUENCY HARMONICS & SYNCHROTRON SIDE BANDS

- -CONTEXT
- -MOTIVATION
- -BACKGROUND
- ***OBJECTIVE***
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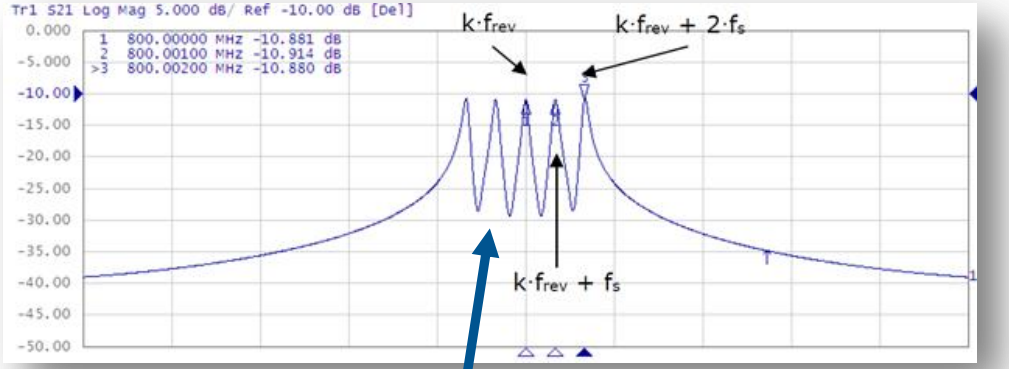
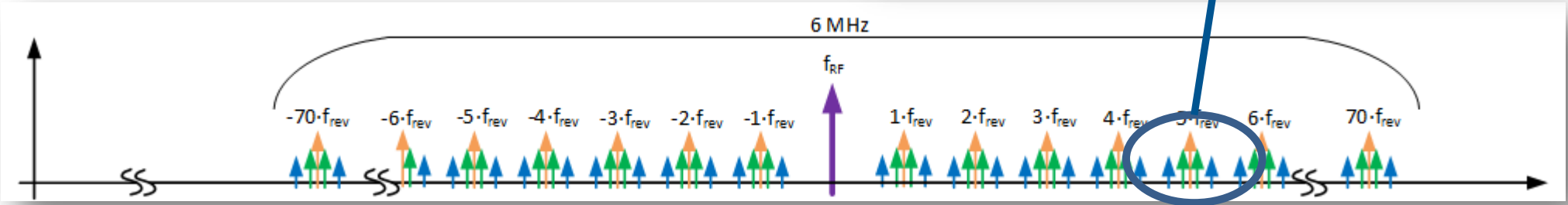
WIDE BAND BEAM SYNCHRONOUS PROCESSING

$f_{RF} + kf_{rev}$ Transient Beam Loading

$f_{RF} + kf_{rev} \pm f_s$ Stability dipolar mode

$f_{RF} + kf_{rev} \pm 2f_s$ Stability quadripolar mode





h 4620	RF Freq. [MHz]	Rev Freq. [KHz]	Synch. Freq. [Hz]
Injection	~ 199.550	~ 43.27	~ 1000
Extraction	~ 200.3946	~ 43.37	~ 300

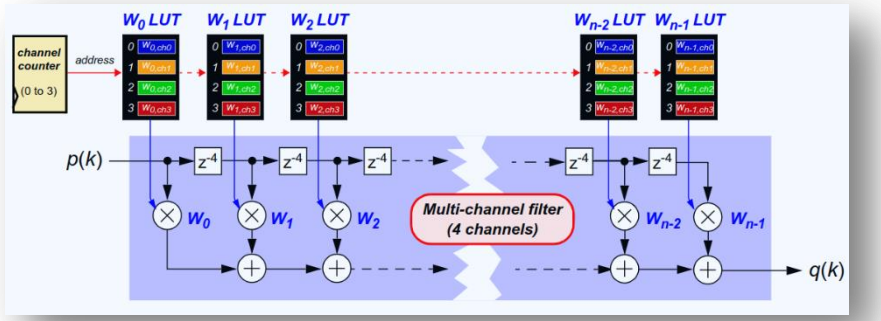
REGULATION BW +/- 3 MHz
(approx. 70 frev single side)

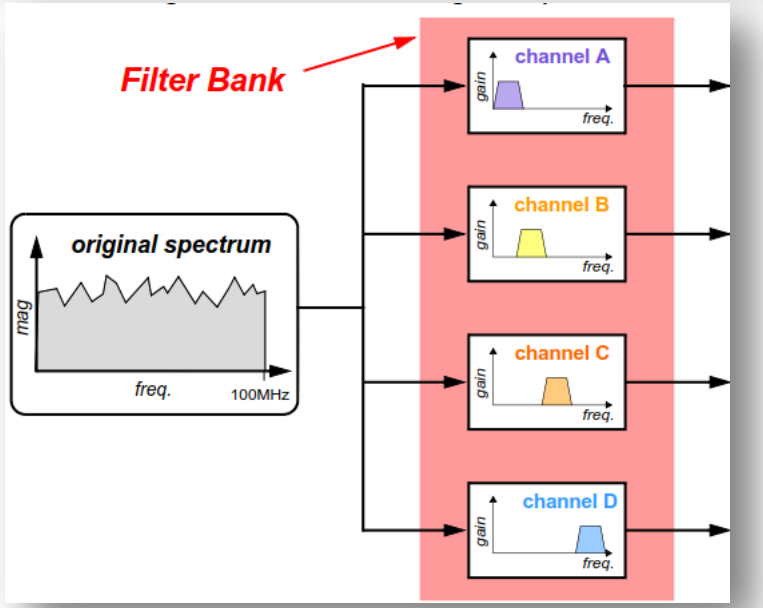
CAVITY BW 0.7 MHz @ -3db

Fixed f_{samp}
Adapt filter to f_{rev}

SOLUTION SPACE EXPLORATION…

RECONFIGURABLE MULTI-HARMONIC FILTER, BANK OF FILTERS…





B Field ramp; $\frac{dRF}{dt} \approx 2\ MHz/s$

Regulation BW $\approx 3\ MHz \rightarrow$ worst k·f_{rev} at k = 70

k=1 $\rightarrow \frac{df_{rev}}{dt} \approx 430\ Hz/s$

k=70 $\rightarrow \frac{df_{rev}}{dt} \approx 30\ KHz/s$

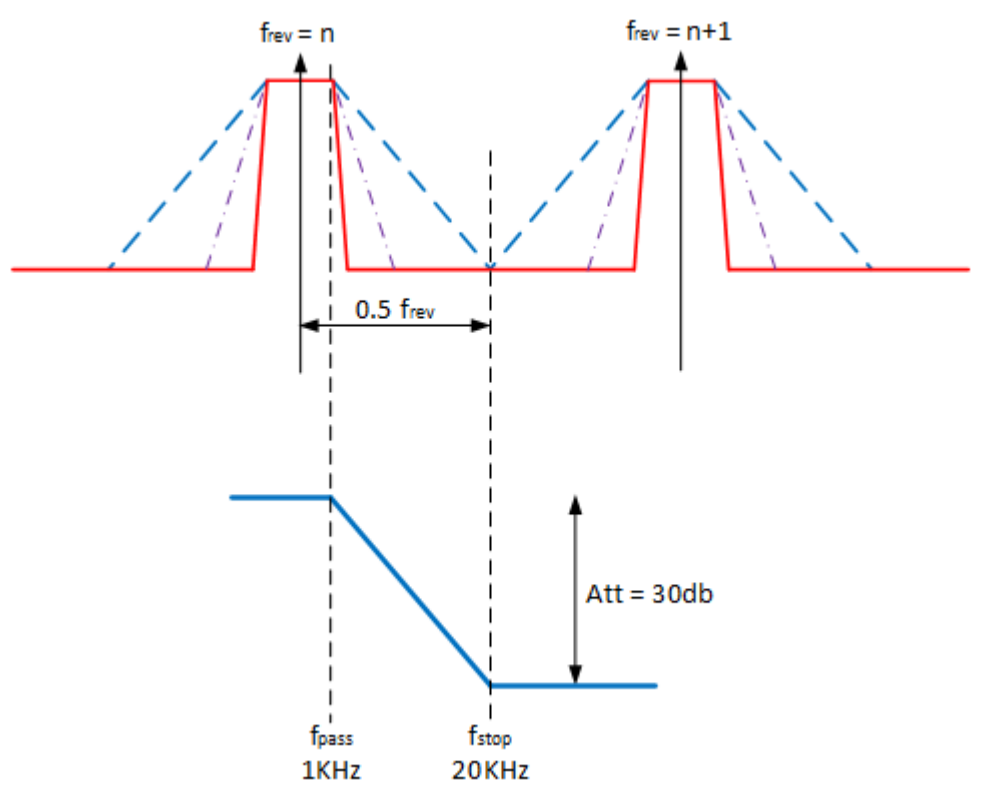
Filter BW = 200 Hz

Update when f_{rev} varies 10% of filter BW (20Hz)

Worst Update rate of 0.6 mS – 1.5Kupdates/s

SOLUTION SPACE EXPLORATION…

SINGLE HARMONIC PROTOTYPE FILTER EVALUATION…



FIR FILTER;

Sampling @ 40Msps
Astop = 30db
Fpass = 1KHz
Fstop = 20KHz ($f_{rev}/2$)

FIR of aprox 2400 taps
Group delay @ 40 MSps 30 us
PROBLEM AS T_{rev} IS 23 us

IIR FILTER;

SAME BRUT FORCE APPROACH…
REDUCTION OF STABILITY MARGINS

SOLUTION SPACE EXPLORATION…

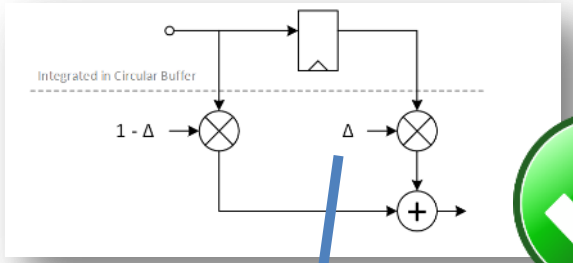
VARIABLE IIR BASED IN FRACTIONAL DELAY REGISTERS

- -CONTEXT
- -MOTIVATION
- -BACKGROUND
- -OBJECTIVE
- ***SOLUTIONS***
- -WRAP UP
- -YOUR TIME…

IMPLEMENTATION OF BOUSSARD IDEA WITH DIGITAL SYNCH. DESIGN

IIR homothesis resides in delay between samples (sampling time)

FRACTIONAL (SAMPLING TIME) DELAY REGISTER



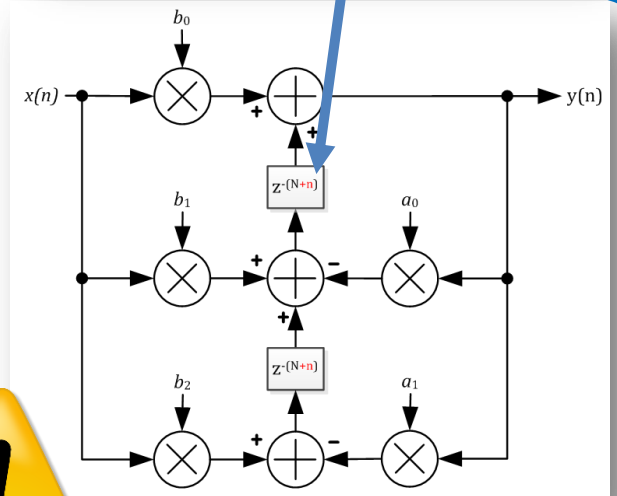
BIQUAD IMPLEMENTATION

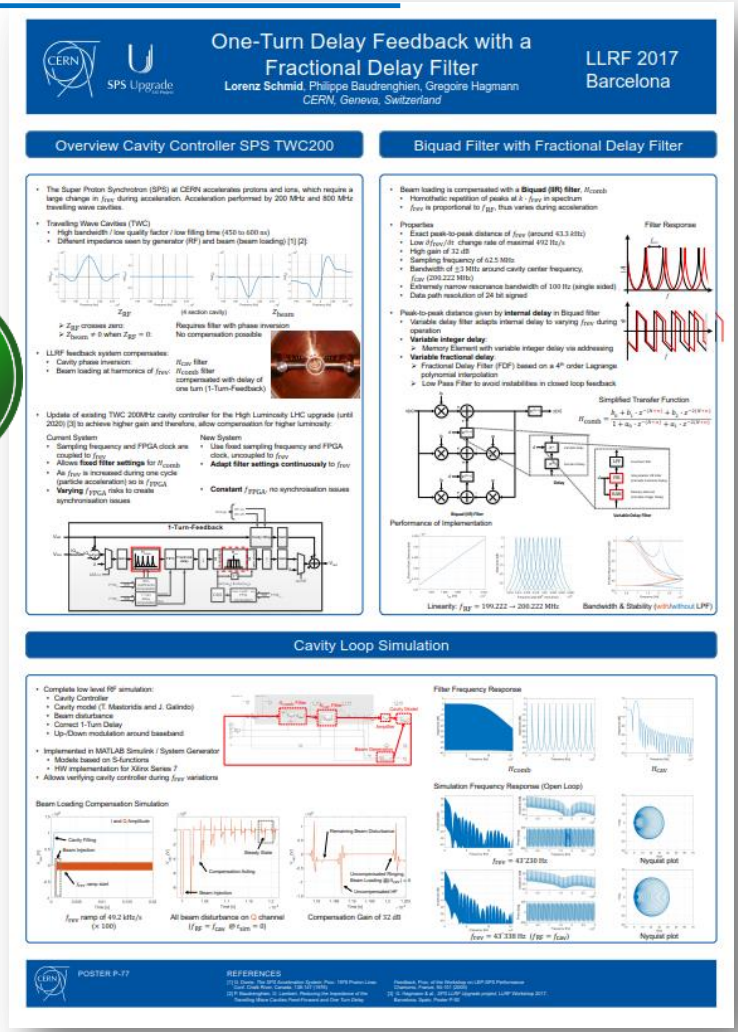
$$H_{\text{comb}} = \frac{b_0 + b_1 \cdot z^{-(N+n)} + b_2 \cdot z^{-2(N+n)}}{1 + a_0 \cdot z^{-(N+n)} + a_1 \cdot z^{-2(N+n)}}$$

N: Integer Delay

n: Fractional Delay (varies run-time)

Ad-hoc OTFB solution





SOLUTION SPACE EXPLORATION…

INSTEAD OF MOVING THE FILTER (DPS) TOWARDS DATA…
"BRING DATA TOWARDS FILTERS"

A DYNAMIC SPECTRUM "HOMOTHER"; *RESAMPLER*

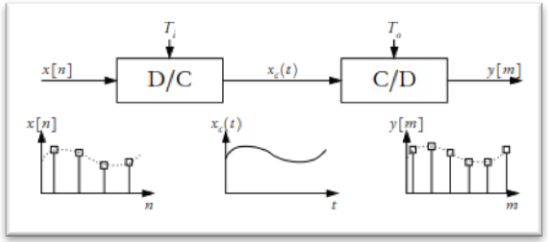
CD
44.1 kHz

MPEG-1
32 KHz 44.1 KHz 48 kHz

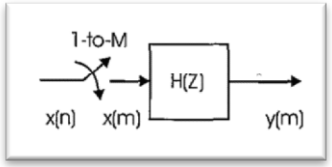
STATIC RATIO RESAMPLERS
FIXED (always same ratio) OR VARIABLE (several ratios);
Audio, Radar, Modems

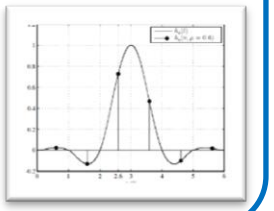
Current work;
Architectural exploration of the idea

ANALOG INTERPRETATION OF A RESAMPLER



DISCRETE INTERPRETATION OF A RESAMPLER





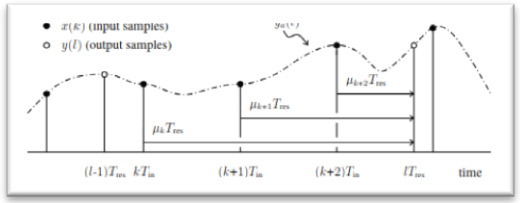
- Interpolation between samples
- Delay of samples

Following Images taken from: "*Multirate Signal Processing for Communication Systems*", Fred Harris

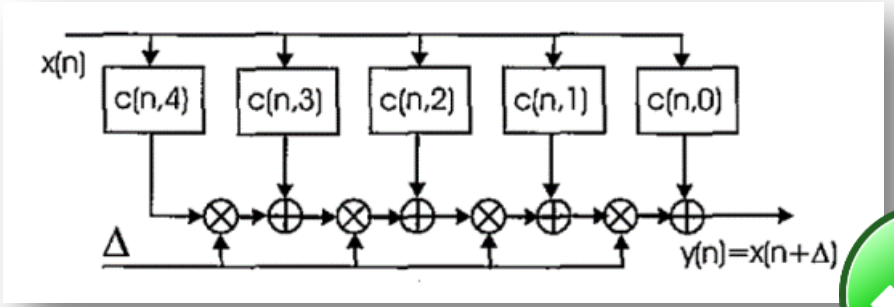
UPSAMPLER IMPLEMENTATION

VARIABLE FRACTIONAL DELAY & CONTROL LOGIC TO COMPUTE DELAY

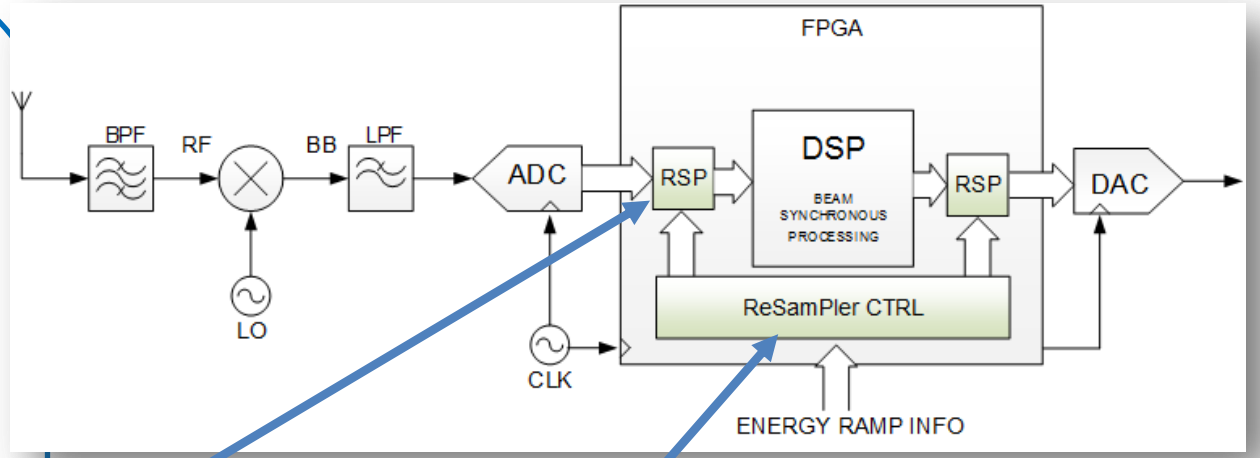
FARROW ARCHITECTURE



- Polyphase decomposition of reconstruction shifted filter (static)
- Coefficients approximated by polynomials
- Reshuffle polynomials and filter architecture to obtain a Taylor series representation of the desired output



PARAMETERS; input and delay



PHASE ACCUMULATORS

- Real time computation of the delay for arbitrary sampling rate conversion
- Difference of two phase accumulators at input and output rate

WRAP UP

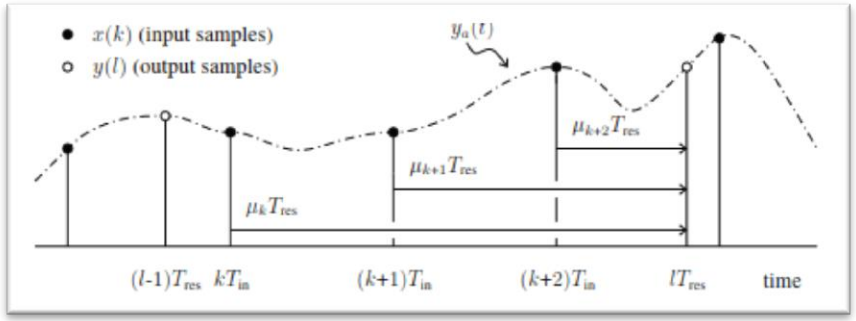
- MOVE FROM CLASSICAL RF DISTRIBUTION TO LOCAL REGENERATION
- MOVE FROM RF DERIVED CLOCK TO FIXED REGENERATED CLOCK
- TEST SUITABILITY OF THIS APPROACH FOR BEAM SYNCHRONOUS PROCESSING
- IMPLEMENTATION OF THE OTFB ALGORITHM BASED ON FIXED CLOCK
  - AD-HOC IMPLEMENTATION WITH BIQUAD AND FRACTIONAL DELAY
  - GENERIC IMPLEMENTATION WITH A RESAMPLER FOR HOMOTHETIC TRANSFORMATION USED IN BEAM SYNCHRONOUS PROCESSING

THANK YOU

Your Time…

BACK UP SLIDES

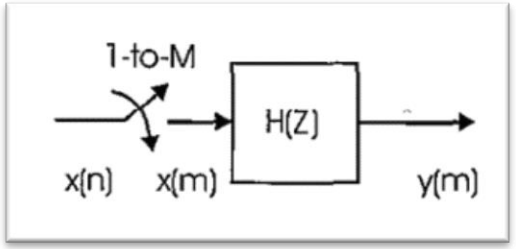
RESAMPLER



COMPUTATION OF NEW SAMPLES;

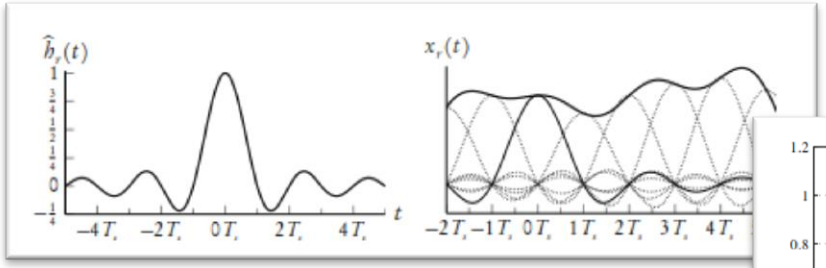
- INTERPOLATION BETWEEN AVAILABLE SAMPLES
- VARIABLE FRACTIONAL DELAY OF AVAILABLES

UP-SAMPLER AS EXAMPLE

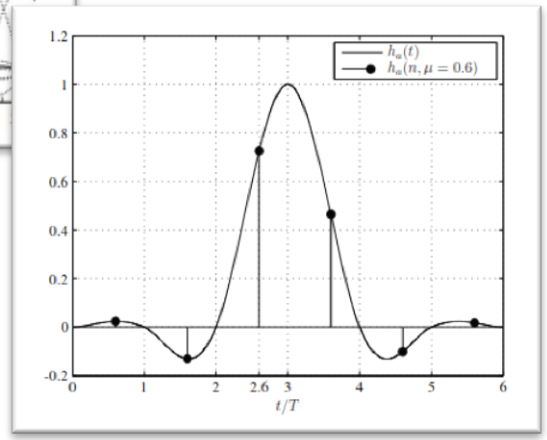


Zero value sample insertion and filtering to recover information

CLASSIC APPROACH, NO CIC OR OTHER



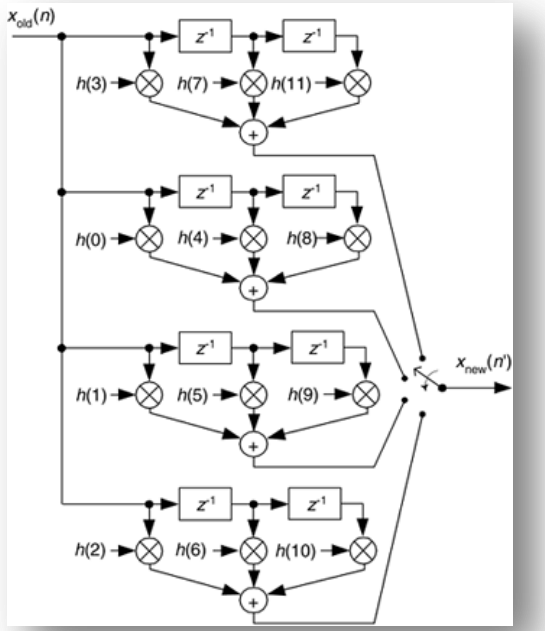
Apply delay by shifting impulse response, windowing



UPSAMPLER IMPLEMENTATION

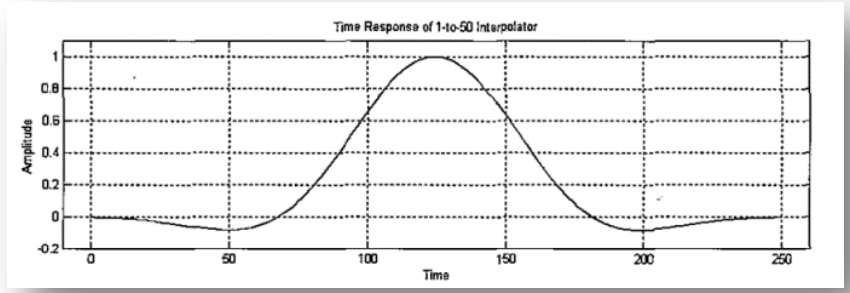
FARROW ARCHITECTURE

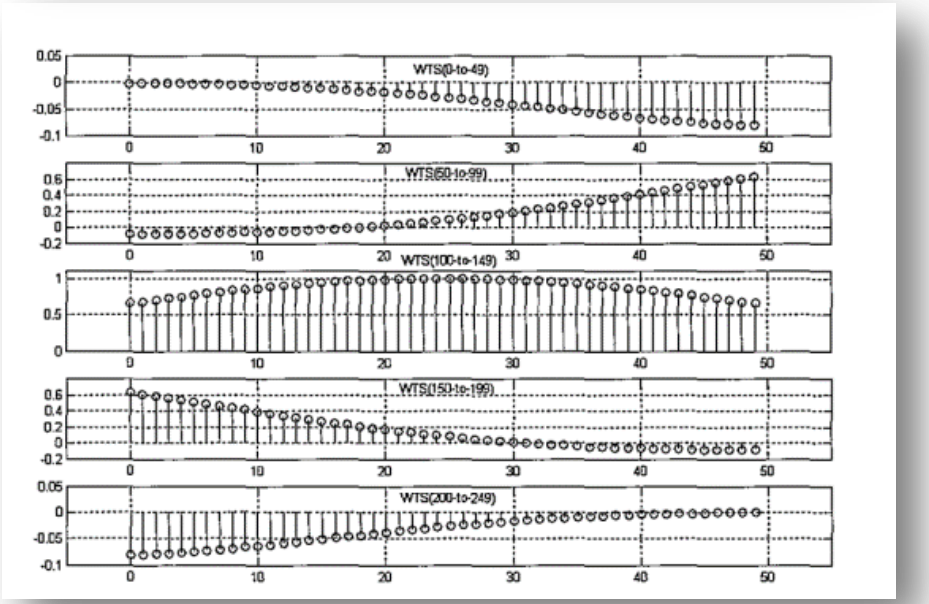
POLYPHASE DECOMPOSITION OF DELAY FILTER



Each branch provides a delayed sample by 1/P of the input sample interval

Equivalent to decompose the impulse response of the filter in segments mapped to the coefficient columns of the subfilters





Original 250 tap filter split in 50 branches of 5 taps

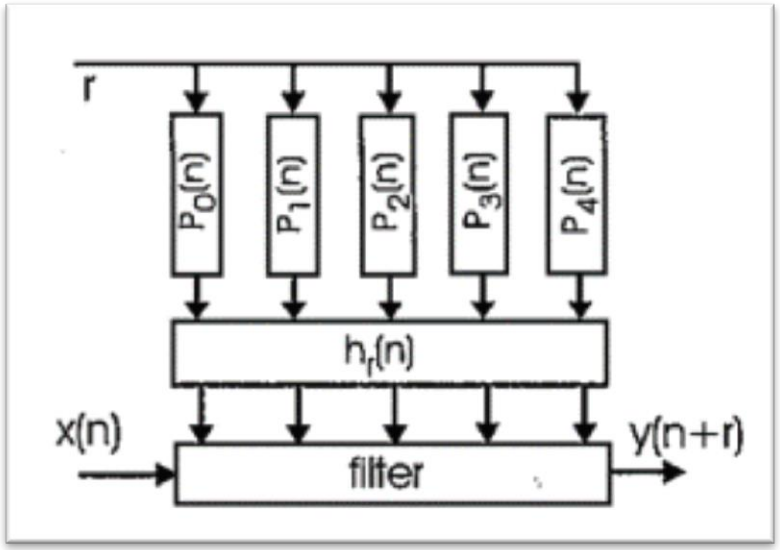
UPSAMPLER IMPLEMENTATION

-CONTEXT
-MOTIVATION
-BACKGROUND
-OBJECTIVE

SOLUTIONS

-WRAP UP
-YOUR TIME…

APROXIMATE THE SEGMENTS WITH A LOW ORDER POLYNOMIAL



With some further maths, it is possible to reorganize polynomials and the filter…
We obtain a Taylor series representation of the desired output with the input and delay as only parameters

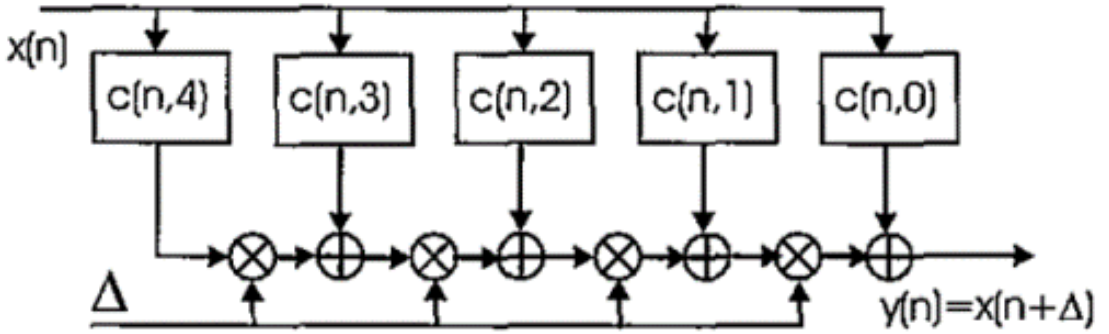
- No need to store coefficient storage, only polynomials
- Evaluation of the polynomials at desired delay value gives coefficient, implicit interpolation of coefficient

$$y(n+\Delta) = c_0(x) + c_1(x)\cdot\Delta + c_2(x)\cdot\Delta^2 + c_3(x)\cdot\Delta^3 + c_4(x)\cdot\Delta^4$$

UPSAMPLER IMPLEMENTATION

FINALLY, USE HORNER RULE TO EFFICIENTLY IMPLEMENT IT

$$y(\Delta) = c_0 + c_1\Delta + c_2\Delta^2 + c_3\Delta^3 + c_4\Delta^4$$
$$= c_0 + \Delta\cdot(c_1 + \Delta\cdot(c_2 + \Delta\cdot(c_3 + \Delta\cdot c_4)))$$



Farrow architecture

UPSAMPLER IMPLEMENTATION

VARIABLE FRACTIONAL DELAY & CONTROL LOGIC TO COMPUTE DELAY

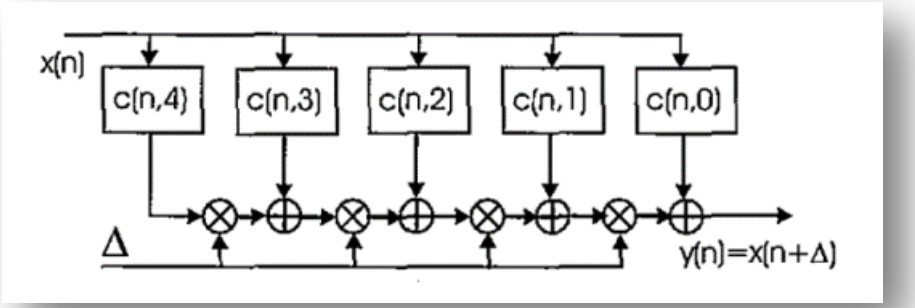
-CONTEXT
-MOTIVATION
-BACKGROUND
-OBJECTIVE

SOLUTIONS

-WRAP UP
-YOUR TIME…

FARROW ARCHITECTURE

- Polyphase decomposition of reconstruction shifted filter (static)
- Coefficients approximated by polynomials
- Reshuffle polynomials and filter architecture to obtain a Taylor series representation of the desired output



PARAMETERS; input and delay

PHASE ACCUMULATORS

- Delay is the difference between two counters, phase accumulators
- One running at input sampling rate
- Second running at output sampling rate
- Real time computation of the delay for arbitrary sampling rate conversion