

Beam Synchronous Processing: Fixed Clock and RF Regeneration. New Paradigms for CERN SPS LLRF

LLRF 2017



UNIVERSITAT POLITÈCNICA
DE CATALUNYA
BARCELONATECH



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UPGRADES & NEW PROJECTS



High Luminosity LHC

Beam Synch. Processing
One Turn Feedback



Beam loading
Cavity impedance



Distance or Time of flight
Clock Synchronization
RF Distribution



High Tech SoC
Deterministic Networks
Standards uTCA



IMPLICATION OF NEW ALGORITHMS ?
NEW TECHNOLOGIES ?

Higher Beam Current



Machine Scaling



CONTEXT

- MOTIVATION
- BACKGROUND
- OBJECTIVE
- SOLUTIONS
- WRAP UP
- YOUR TIME...



ARE NEW TECHNOLOGIES FOR US?

PROMISING RF DISTRIBUTION AND SYNCHRO.

CONTEXT

- Classic **distribution** of RF
- Clock recovery **from the RF**

- Local **Regeneration** of RF
- Use of **Deterministic Link** for FTW and phase distribution
- Clock **extraction from data stream** of deterministic link



RECALL: RF OF CERN SYNCHROTRON'S IS RAMPED

(energy increase)

- **Sweeping clock** for electronics
- **Custom** and NIM / VME modules

- **Fixed clock**
- **uTCA**



BEAM SYNCHRONOUS PROCESSING WITH FIX CLOCK DEMONSTRATOR: ONE TURN FEEDBACK ALGORITHM

SPS 200 MHz LLRF CAVITY CONTROLLER

The collage consists of several technical documents from the SPS LLRF Upgrade project. The top document is the 'SPS LLRF Upgrade project' overview, listing the project name, location (Barcelona), and team members (Grigoris Hagmann, Philipp Bauchhag, J. Galindo, G. Kotzian, L. Schmidt, A. Späumer). Below it are four main sections: 'SPS RF Upgrade as HL-LHC injector' (discussing beam performance requirements and the need for a new RF system), 'Fixed-frequency sampling & White-rabbit' (describing the sampling method and its benefits), 'SPS 200MHz Cavity-controller' (detailing the design of the cavity controller and its integration with the White-rabbit system), and 'SPS LLRF Architecture' (showing the overall system architecture). The bottom section, 'uTCA platform', describes the hardware and software used for the upgrade.

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DISTRIBUTED ARCHITECTURE

	Clock extracted from RF	Dedicated clock distribution
-CONTEXT CLOCK INTERRUPTION BETWEEN CYCLES	Periodic resynchronizations require RF interruptions, which induces clock interruption in electronics	Dedicated clock can independently handle RF generation and DSP processing
MOTIVAT. -BACKGROUND -OBJECTIVE -SOLUTIONS -WRAP UP -YOUR TIME...	Beam Phase Loop continuously modulates RF on top of sweep Cleaning PLL architectures at specific frequencies Spectral purity of reconstructed clock not optimal Beam parameters relying on the RF noise	Dedicated cleaning architecture for clock Optimal spectral purity Optimal beam parameters
RF GYMNASTICS	Manipulations of the RF parameters. Slip stacking merging bunches in the phase space will not be possible. Fast or abrupt modifications of the phase or frequency of the RF complicated as it affects the ADC-DAC-FPGA clocking	Dedicated clock for DDS enables Digital RF regeneration Instantaneous modifications of RF phase and frequency driven by data, not by clocks Any type of RF gymnastics

FIXED CLOCK

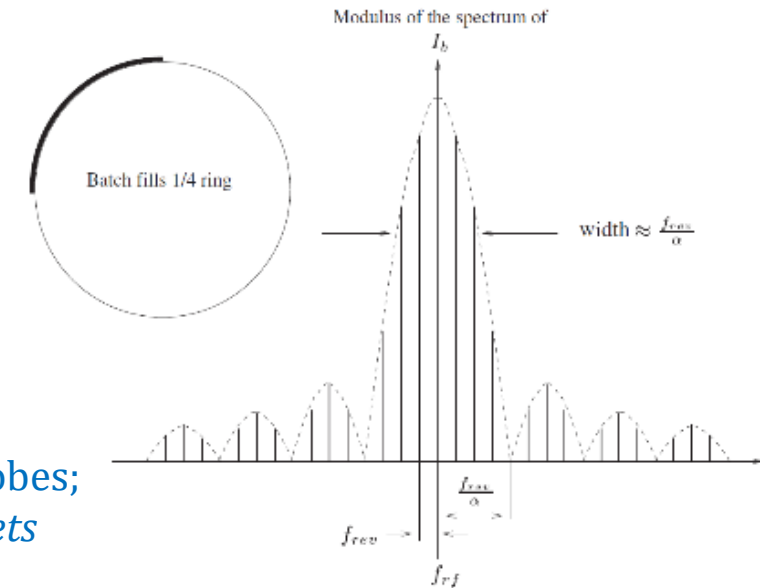
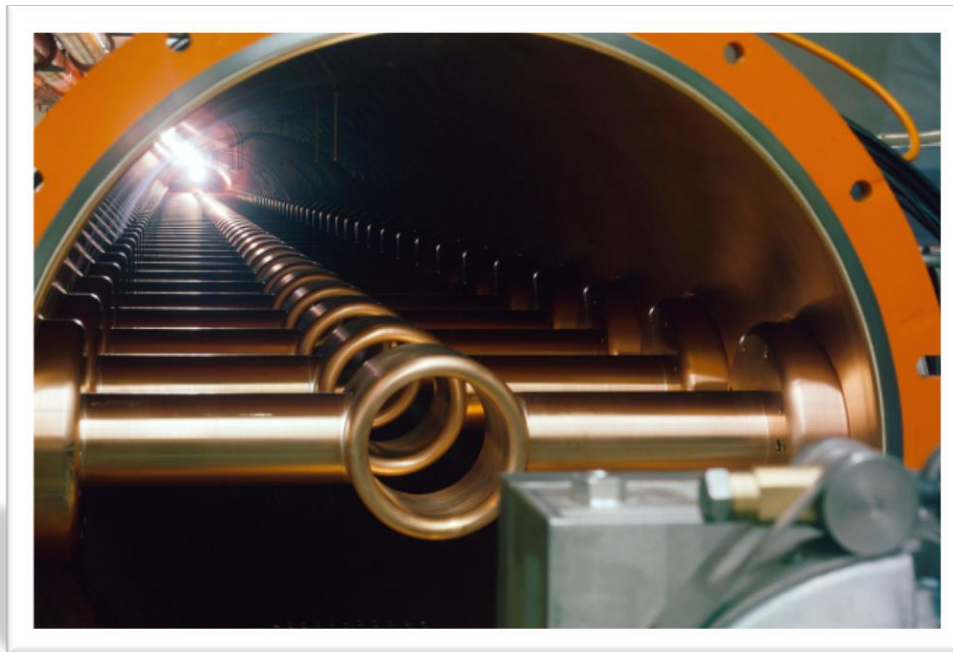
	Swept Clock	Fixed Clock
-CONTEXT	Variable sampling clock → Variable loop delay Compromise in Regulation Bandwidth and Feedback Stability	Fixed sampling clock → Fixed loop delay Optimal Regulation Bandwidth and Feedback Stability
MOTIVAT.	RF as harmonic of clock → multiplexing required to cover wide RF range Phase Jumps when multiplexing	Simple DDS implementation can cover a wider range without interruption
-BACKGROUND	Complex analogue reconstruction filter Coherent signals fall in swept range Non optimal integrated noise	Fixed analogue reconstruction filters Coherent signals at fixed digital frequencies Optimized integrated noise
-OBJECTIVE		
-SOLUTIONS		
-WRAP UP	Lower spectral purity of clock → DDS and IQ sensitive to jitter → Problem for heterodyne architectures	Non IQ sampling and Direct down conversion easier
-YOUR TIME...		
	PLLs tracking and locking Max dF/dt for DCM in FPGAs Clock domain synchronization Complex PAR constraints Serial interfaces FIFOs	PLLs and DCM readily usable Easy place and route Ease clock domain synchronization Ease use of serial interfaces and modern technologies

WHAT IS BEAM LOADING?

Interaction between beam and accelerating cavity
Beam induces an EM field **perturbing** desired cavity one
Effective accelerating voltage;
vector sum of RF generator voltage
and the beam-self-induced voltage

Stationary; f_{RF}

Transient; $f_{RF} + n f_{rev}$



Revolution frequency lobes;
Irregular filling of buckets

Single line at RF frequency;
Bunch spacing multiple of the RF period, assuming that the bunch frequency is much larger than bandwidth of cavity

-CONTEXT
-MOTIVATION

BACK
GROUND

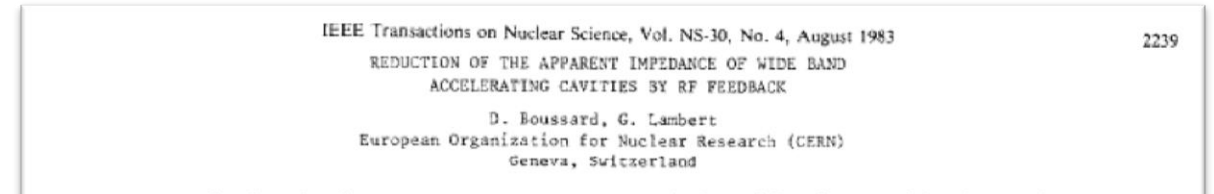
-OBJECTIVE
-SOLUTIONS
-WRAP UP
-YOUR TIME...

AND THE ONE TURN FEEDBACK?

OTFB algorithm is a very old innovation at CERN, SPS Implementation

TRANSIENT BEAM LOADING

$$f_{RF} + kf_{rev}$$



Reduction Of The Apparent Impedance Of Wide Band Accelerating Cavities By RF Feedback, BOUSSARD 1983

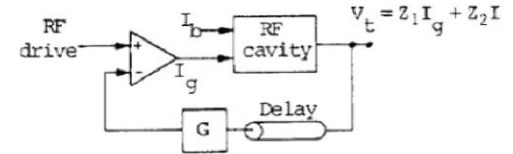
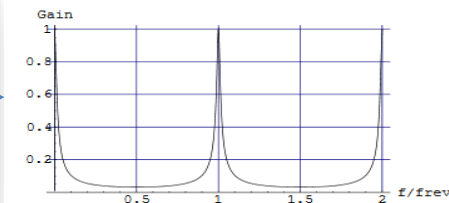
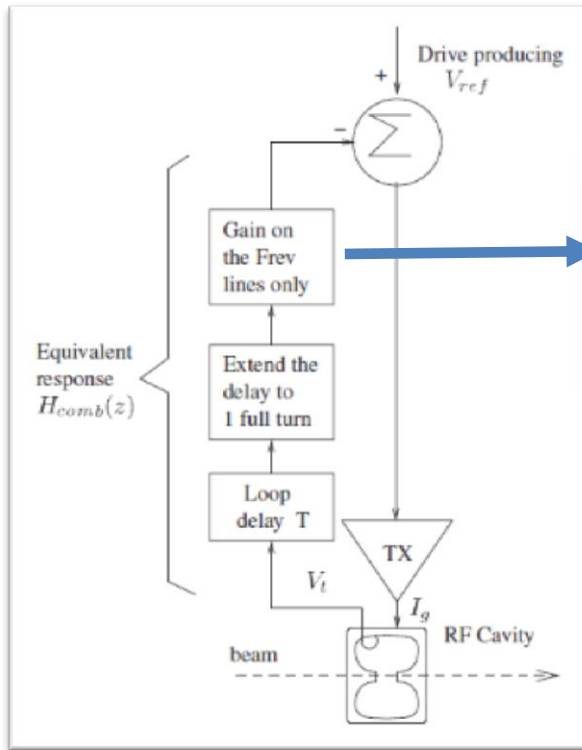


Fig. 1 Principle of the RF feedback

-CONTEXT
 -MOTIVATION

BACK
 GROUND

-OBJECTIVE
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$$H(z) = \frac{1}{1 - az^{-N}}$$

WIDE BAND
 BEAM SYNC. PROCESSING

TODAY'S IMPLEMENTATION

Patches to the original design
 Custom digital module
 Discrete components...

Fig. 4 The digital filter and delay



DO WE MISS SOMETHING?

SWEPT CLOCK...

WHAT DOES IT MEAN?

-CONTEXT
-MOTIVATION

BACK
GROUND

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-YOUR TIME...

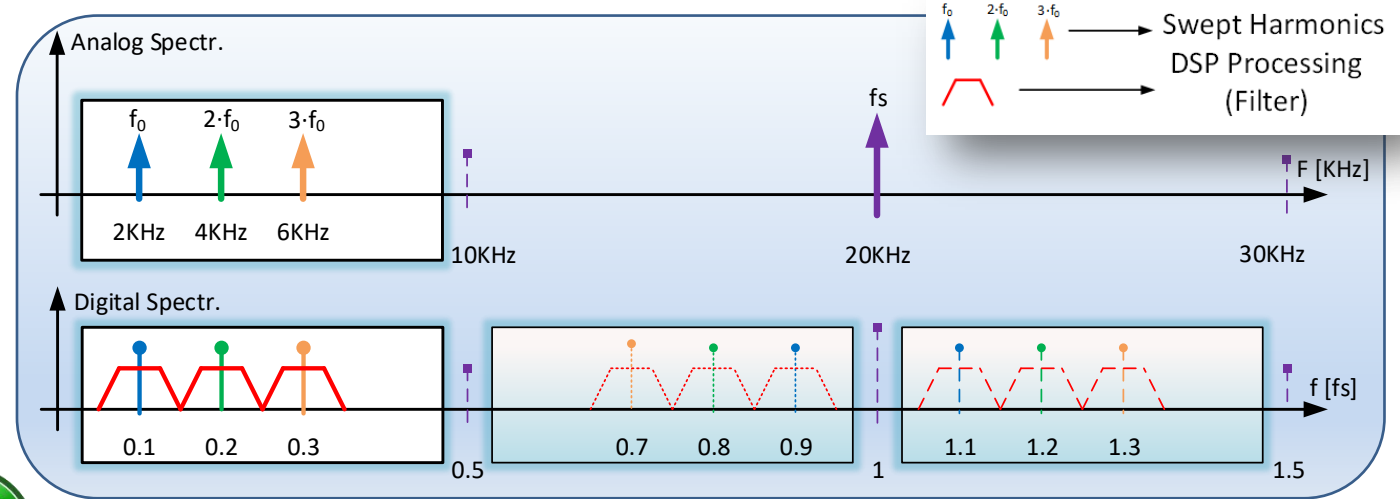
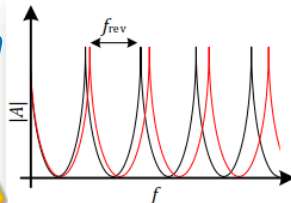
CLASSIC DSP SYSTEM
*Sampling frequency of
ADCs, DACs, FPGAs, DSPs
is FIXED*



DEALING W. HARMONICS
*Beam Synch. Processing
Reconfig. of filters (DSP)*

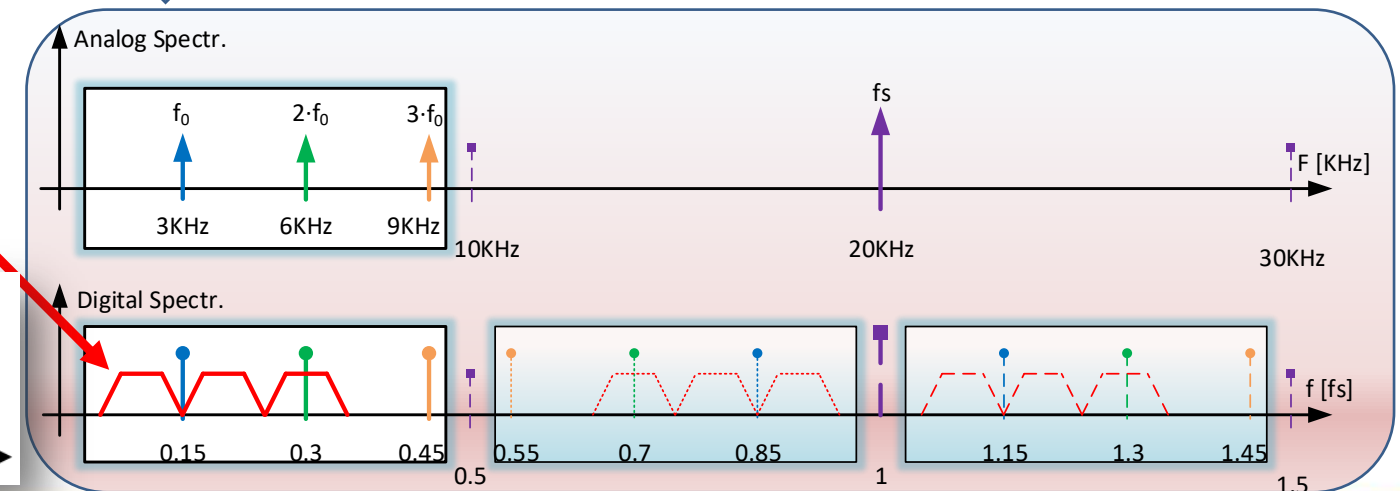
Homothetic transformation

- harmonic position
- harmonic spacing



f_0 : from 2KHz to 3KHz
 f_s : fixed at 20KHz

ENERGY RAMPING...
FREQ MOVING



DO WE MISS SOMETHING?

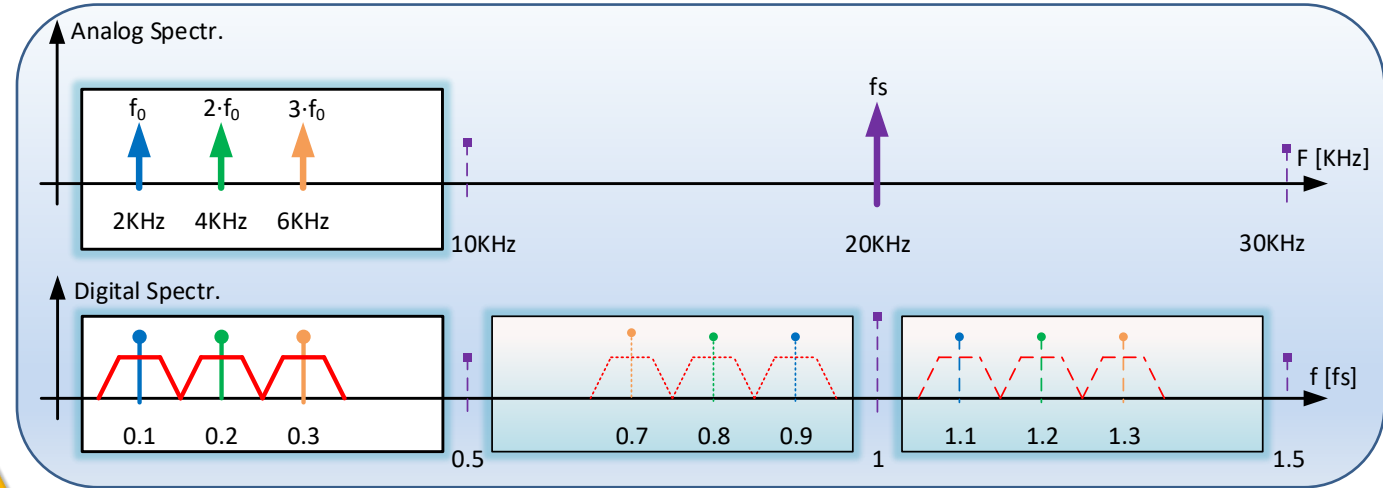
SWEPT CLOCK...

WHAT DOES IT MEAN?

CERN DSP SYSTEM
Sampling frequency of ADCs, DACs, FPGAs, DSPs is SWEPT with RF

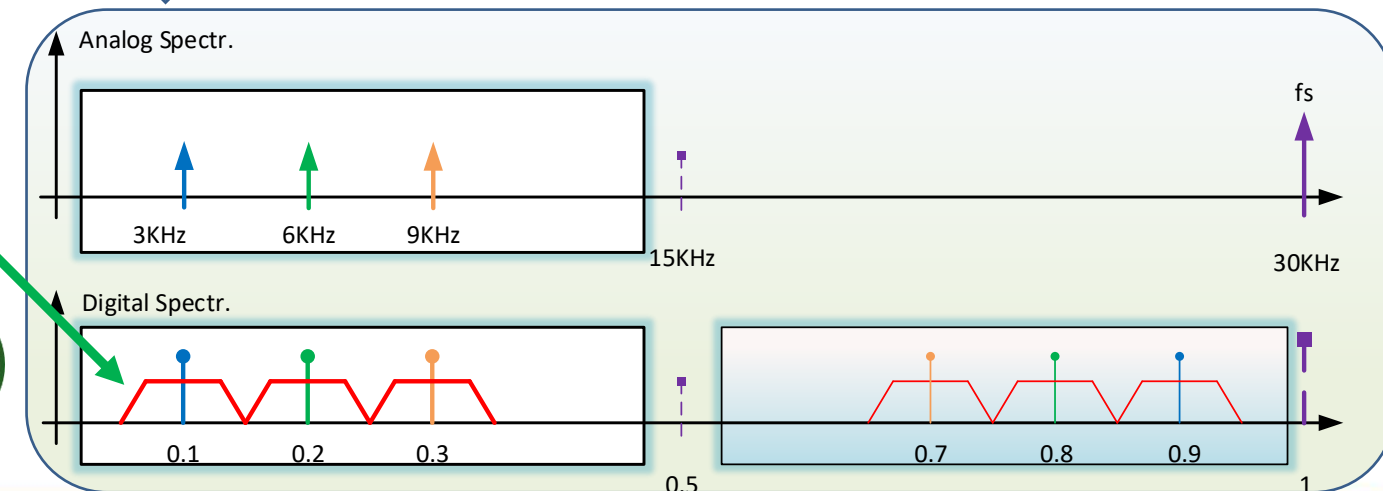


AUTOMATIC HOMOTHESES
Filter (DSP) tracks harmonics
Beam synch. processing
 One Turn Feedback algorithm



f_0 : from 2KHz to 3KHz
 f_s : from 20KHz to 30KHz

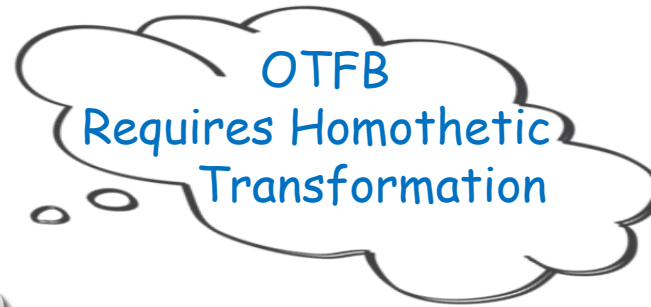
ENERGY RAMPING...
 FREV MOVING



- CONTEXT
- MOTIVATION
- BACK GROUND**
- OBJECTIVE
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CHRISTMAS PRESENT FOR THIS YEAR...

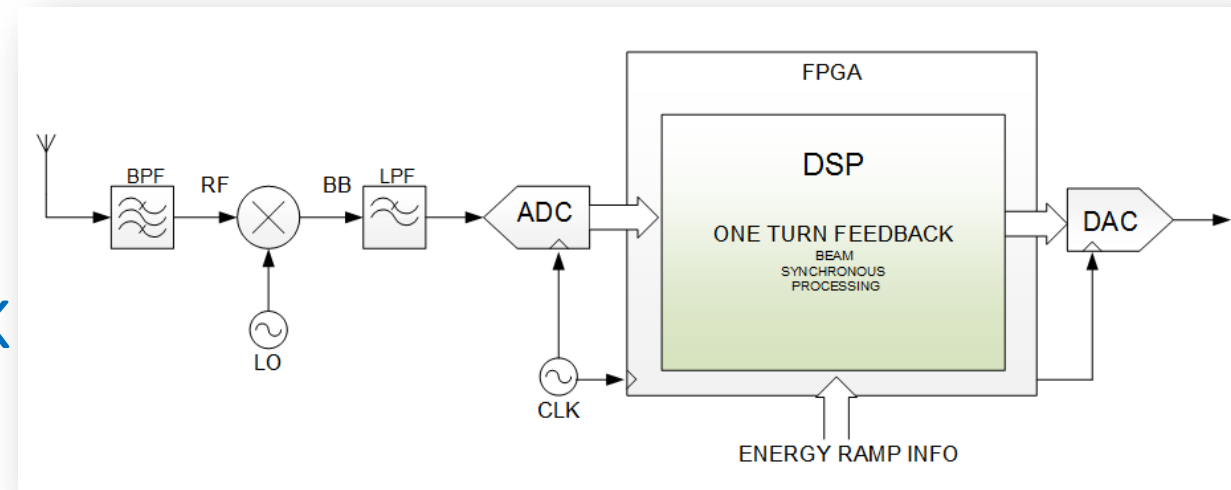
MAY WE HAVE A **PROBLEM** WITH FIXED CLOCKS FOR BEAM SYNCHRONOUS PROCESSING?



MAYBE A NEW FEEDBACK (COMB) FILTERING ARCHITECTURE???



NEW **FIX CLOCK** ARCHITECTURE FOR ONE TURN FEEDBACK ALGORITHM



- CONTEXT
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SPECIFICATION OF THE FILTER

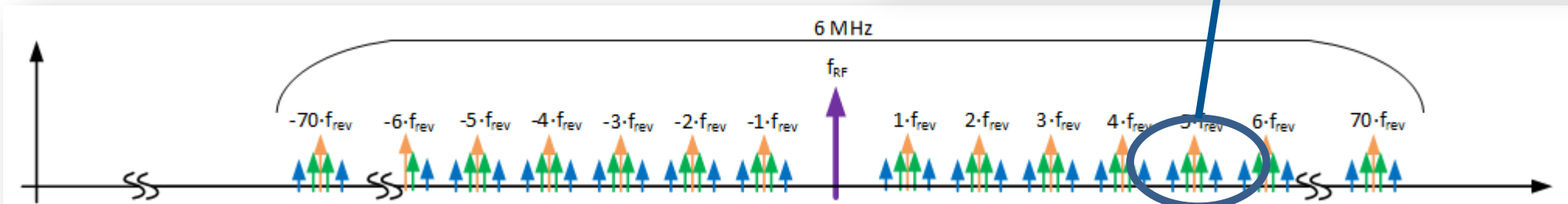
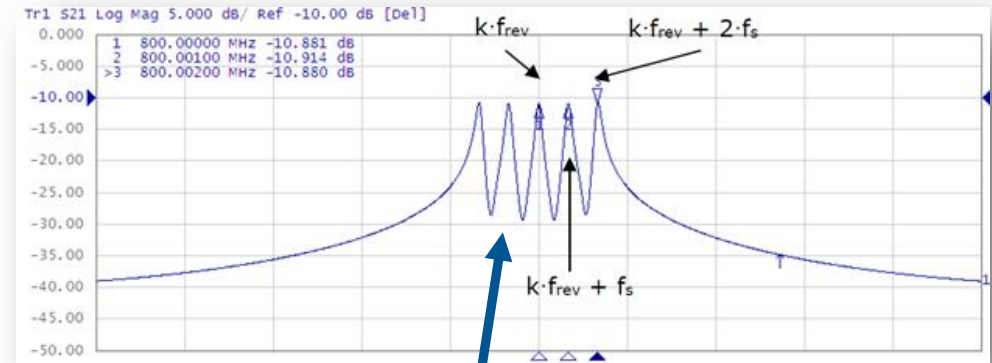
AIM: REVOLUTION FREQUENCY HARMONICS & SYNCHROTRON SIDE BANDS

WIDE BAND BEAM SYNCHRONOUS PROCESSING

$f_{RF} + kf_{rev}$ Transient Beam Loading

$f_{RF} + kf_{rev} \pm f_s$ Stability dipolar mode

$f_{RF} + kf_{rev} \pm 2f_s$ Stability quadripolar mode



h 4620	RF Freq. [MHz]	Rev Freq. [KHz]	Synch. Freq. [Hz]
Injection	~ 199.550	~ 43.27	~ 1000
Extraction	~ 200.3946	~ 43.37	~ 300

REGULATION BW +/- 3 MHz
(approx. 70 frev single side)

CAVITY BW 0.7 MHz @ -3db

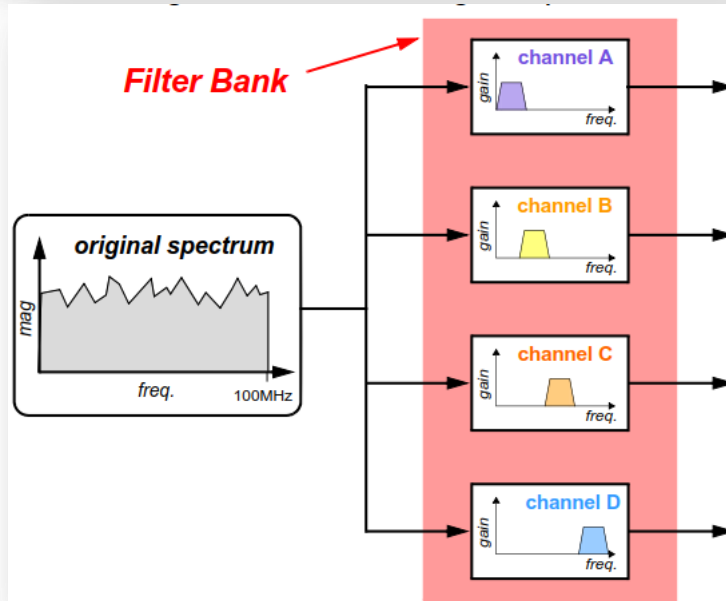
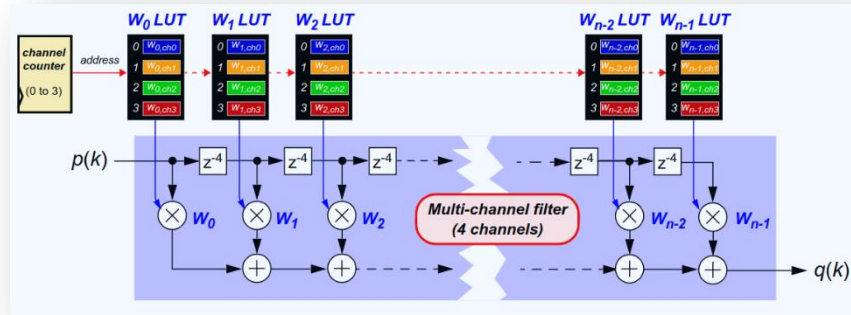
Fixed f_{samp}
Adapt filter to f_{rev}

- CONTEXT
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SOLUTION SPACE EXPLORATION...

RECONFIGURABLE MULTI-HARMONIC FILTER, BANK OF FILTERS...



B Field ramp; $\frac{dRF}{dt} \approx 2 \text{ MHz/s}$

Regulation BW $\approx 3 \text{ MHz} \rightarrow$ worst $k \cdot f_{rev}$ at $k = 70$

$$k=1 \rightarrow \frac{df_{rev}}{dt} \approx 430 \text{ Hz/s}$$

$$k=70 \rightarrow \frac{df_{rev}}{dt} \approx 30 \text{ KHz/s}$$

Filter BW = 200 Hz

Update when f_{rev} varies 10% of filter BW (20Hz)

Worst Update rate of 0.6 mS – 1.5Kupdates/s

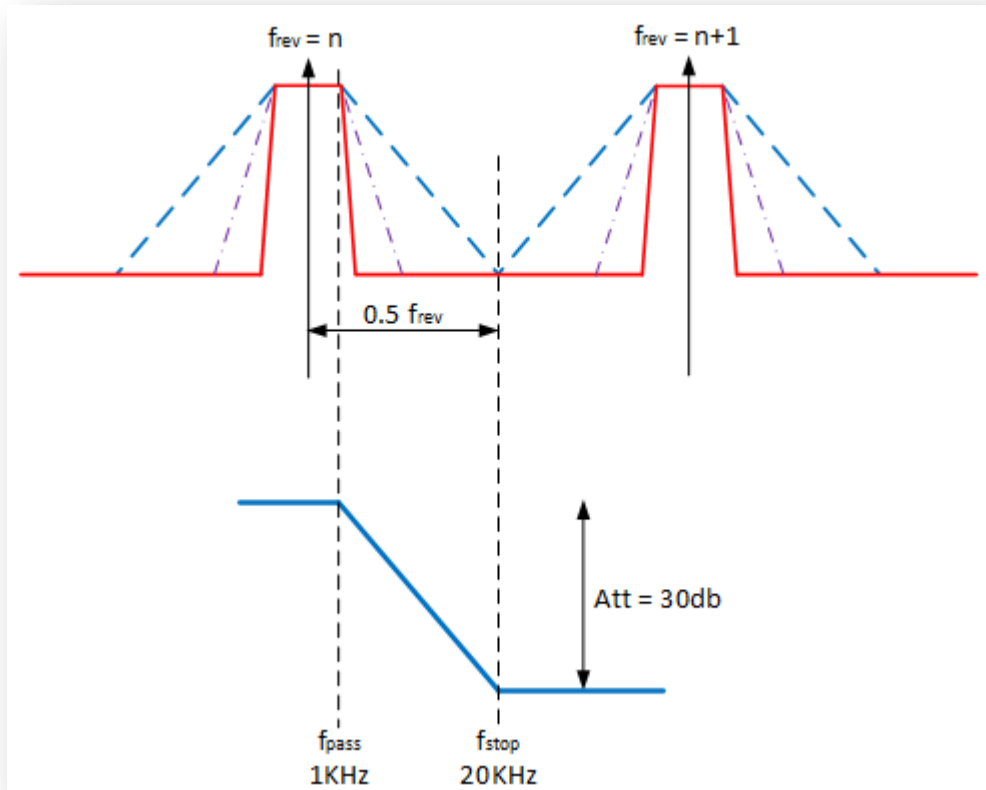
- CONTEXT
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SOLUTIONS

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SOLUTION SPACE EXPLORATION...

SINGLE HARMONIC PROTOTYPE FILTER EVALUATION...



FIR FILTER;

Sampling @ 40MSPs

$A_{stop} = 30 \text{ db}$

$F_{pass} = 1 \text{ KHz}$

$F_{stop} = 20 \text{ KHz} (f_{rev} / 2)$

FIR of aprox **2400 taps**
Group delay @ 40 MSPs **30 us**
PROBLEM AS T_{rev} IS 23 us

IIR FILTER;

SAME BRUT FORCE APPROACH...
REDUCTION OF STABILITY MARGINS



- CONTEXT
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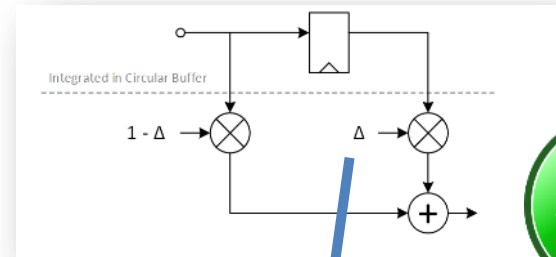
SOLUTION SPACE EXPLORATION...

VARIABLE IIR BASED IN FRACTIONAL DELAY REGISTERS

IMPLEMENTATION OF BOUSSARD IDEA WITH DIGITAL SYNCH. DESIGN

IIR homothesis resides in delay between samples (sampling time)

FRACTIONAL (SAMPLING TIME) DELAY REGISTER



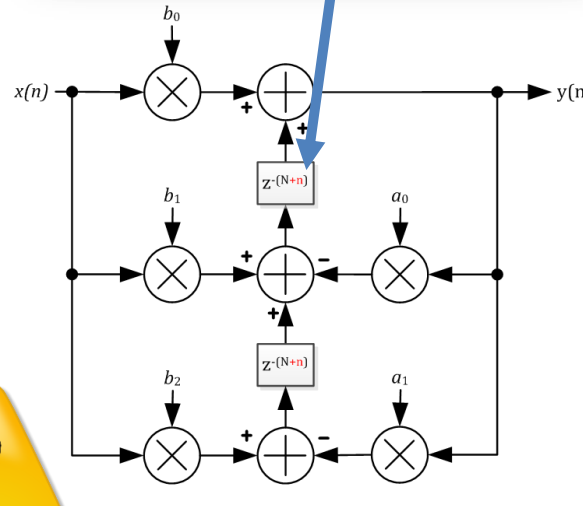
BIQUAD IMPLEMENTATION

$$H_{comb} = \frac{b_0 + b_1 \cdot z^{-(N+n)} + b_2 \cdot z^{-2(N+n)}}{1 + a_0 \cdot z^{-(N+n)} + a_1 \cdot z^{-2(N+n)}}$$

N: Integer Delay

n: Fractional Delay (varies run-time)

Ad-hoc OTFB solution



One-Turn Delay Feedback with a Fractional Delay Filter
Lorenz Schmid, Philippe Baudrenghien, Gregoire Hagmann
CERN, Geneva, Switzerland

LLRF 2017
Barcelona

Overview Cavity Controller SPS TWC200

- The Super Proton Synchrotron (SPS) at CERN accelerates protons and ions, which require a large change in f_{rev} during acceleration. Acceleration performed by 200 MHz and 800 MHz traveling wave cavities.
- Traveling Wave Cavities (TWC)
 - High bandwidth / low quality factor / low filling time (10 to 400 ns)
 - Different impedances seen by generator (RF) and beam (beam loading) [1] [2]
- Z_{TWC} crosses zero:
 - $Z_{TWC} = 0$ when $f_{rev} = 0$: Requires filter with phase inversion. No compensation possible.
- LLRF feedback system compensates:
 - Cavity phase invariance
 - Beam loading at harmonics of f_{rev}
- LLRF feedback system compensates:
 - Memory Element with variable integer delay via addressing
 - Variable fractional delay
 - Fractional Delay Filter (FDF) based on a 4th order Lagrange polynomial interpolation
 - Low Pass Filter to avoid instability in closed loop feedback

Biquad Filter with Fractional Delay Filter

- Beam loading is compensated with a Biquad (BF) filter, H_{comb}
- Hydrostatic repetition of poles at $\pm j\omega$ in spectrum
- f_{rev} is proportional to f_{RF} , thus varies during acceleration

Properties

- Exact peak-to-peak distance of f_{rev} (around 412.1330)
- Low f_{RF}/f_{rev} change rate of maximal 492 Hz/s
- High gain of 32 dB
- Sampling frequency of 62.5 MHz
- Bandwidth of 53 MHz around cavity center frequency, f_{RF} (200.222 MHz)
- Extremely narrow resonance bandwidth of 100 Hz (single sided)
- Data path resolution of 26 bit signed

Filter Response

Peak-to-peak distance given by internal delay in Biquad filter

- Variable delay filter adapts internal delay to varying f_{rev} during operation
- Variable integer delay
- Memory Element with variable integer delay via addressing
- Variable fractional delay
- Fractional Delay Filter (FDF) based on a 4th order Lagrange polynomial interpolation
- Low Pass Filter to avoid instability in closed loop feedback

Simplified Transfer Function

$$H_{comb} = \frac{b_0 + b_1 \cdot z^{-(N+n)} + b_2 \cdot z^{-2(N+n)}}{1 + a_0 \cdot z^{-(N+n)} + a_1 \cdot z^{-2(N+n)}}$$

Performance of Implementation

Linearity: $f_{RF} = 199.222 - 208.222$ MHz

Bandwidth & Stability (with/without LPF)

Cavity Loop Simulation

- Complete low level RF simulation:
 - Cavity Controller
 - Cavity model (T. Meistris and J. Gaskins)
 - Beam disturbance
 - Correct 1-Turn Delay
 - Up-Down modulation around baseband
- Implemented in MATLAB Simulink / System Generator
 - Module based on S-functions
 - HW implementation for Xilinx Series 7
 - Allows verifying cavity controller during f_{RF} variations

Filter Frequency Response

Simulation Frequency Response (Open Loop)

$f_{RF} = 412.1330$ MHz

$f_{RF} = 412.1330$ Hz ($f_{RF} = f_{rev}$)

Beam-Loading Compensation Simulation

f_{RF} ramp of 412.144 Hz/s ($\times 100$)

All beam disturbance on 0 channel ($f_{RF} = f_{RF}$, $\theta_{RF} = 0$)

Compensation Gain of 32 dB

POSTER P-77

REFERENCES

[1] T. Meistris, Ph.D. Thesis, Ecole Polytechnique, Paris, 1993

[2] J. Gaskins, Ph.D. Thesis, Ecole Polytechnique, Paris, 1995

[3] J. Gaskins, Ph.D. Thesis, Ecole Polytechnique, Paris, 1995

[4] J. Gaskins, Ph.D. Thesis, Ecole Polytechnique, Paris, 1995

[5] J. Gaskins, Ph.D. Thesis, Ecole Polytechnique, Paris, 1995

Poster: Beam-Loading Compensation in SPS LLRF

Poster: Beam-Loading Compensation in SPS LLRF

- CONTEXT
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SOLUTION SPACE EXPLORATION...

INSTEAD OF MOVING THE FILTER (DPS) TOWARDS DATA...
“BRING DATA TOWARDS FILTERS”

A DYNAMIC SPECTRUM “HOMOTHER”; RESAMPLER

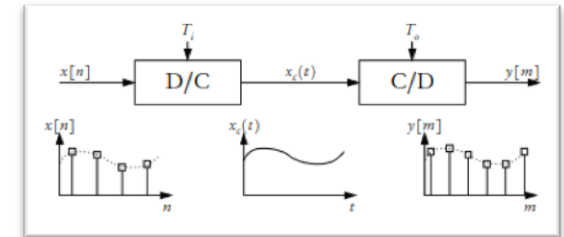


STATIC RATIO RESAMPLERS

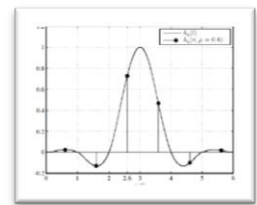
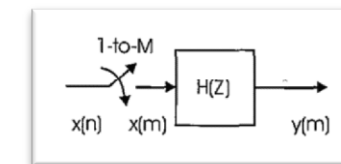
FIXED (always same ratio) OR VARIABLE (several ratios);
Audio, Radar, Modems

Current work;
Architectural exploration of the idea

ANALOG
INTERPRETATION
OF A RESAMPLER



DISCRETE
INTERPRETATION
OF A RESAMPLER



- Interpolation between samples
- Delay of samples

Following Images taken from: “Multirate Signal Processing for Communication Systems”, Fred Harris

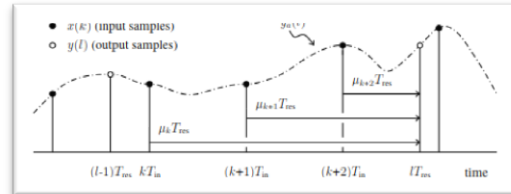
-CONTEXT
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SOLUTIONS

-WRAP UP
-YOUR TIME...

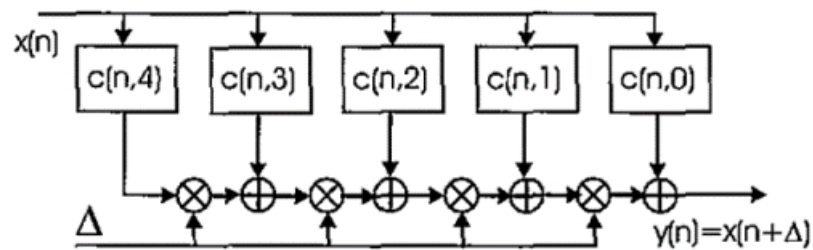
UPSAMPLER IMPLEMENTATION

VARIABLE FRACTIONAL DELAY & CONTROL LOGIC TO COMPUTE DELAY

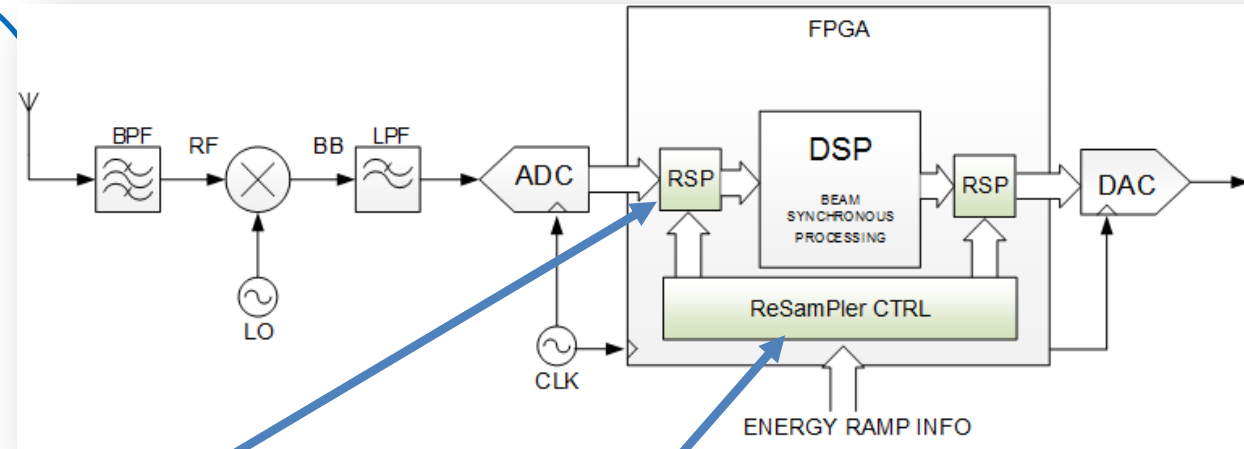
FARROW ARCHITECTURE



- Polyphase decomposition of reconstruction shifted filter (static)
- Coefficients approximated by polynomials
- Reshuffle polynomials and filter architecture to obtain a Taylor series representation of the desired output



PARAMETERS; input and delay



PHASE ACCUMULATORS

- Real time computation of the delay for arbitrary sampling rate conversion
- Difference of two phase accumulators at input and output rate

-CONTEXT
-MOTIVATION
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SOLUTIONS

-WRAP UP
-YOUR TIME...

WRAP UP

- MOVE FROM CLASSICAL RF DISTRIBUTION TO LOCAL REGENERATION
- MOVE FROM RF DERIVED CLOCK TO FIXED REGENERATED CLOCK
- TEST SUITABILITY OF THIS APPROACH FOR BEAM SYNCHRONOUS PROCESSING
- IMPLEMENTATION OF THE OTFB ALGORITHM BASED ON FIXED CLOCK
 - AD-HOC IMPLEMENTATION WITH BIQUAD AND FRACTIONAL DELAY
 - GENERIC IMPLEMENTATION WITH A RESAMPLER FOR HOMOTHETIC TRANSFORMATION USED IN BEAM SYNCHRONOUS PROCESSING

-CONTEXT
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WRAP UP

-YOUR TIME...

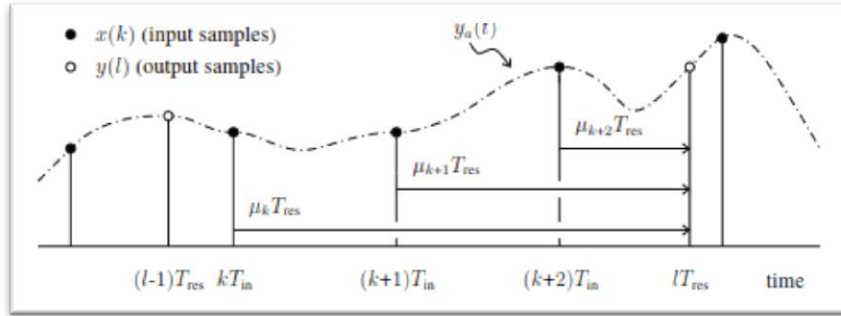
THANK YOU

Your Time...



BACK UP SLIDES

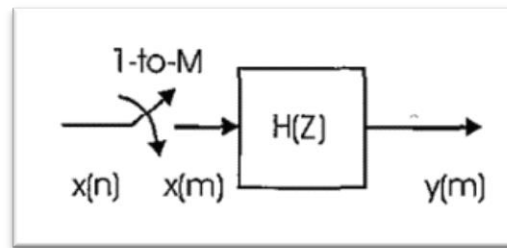
RESAMPLER



COMPUTATION OF NEW SAMPLES;

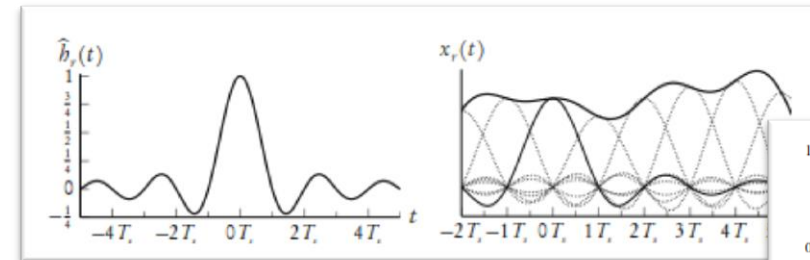
- INTERPOLATION BETWEEN AVAILABLE SAMPLES
- VARIABLE FRACTIONAL DELAY OF AVAILABLES

UP-SAMPLER AS EXAMPLE

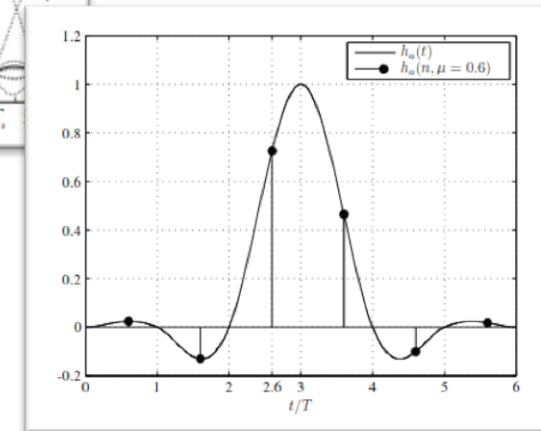


*Zero value sample insertion
and filtering to recover information*

CLASSIC APPROACH, NO CIC OR OTHER



*Apply delay by shifting
impulse response,
windowing*



-CONTEXT
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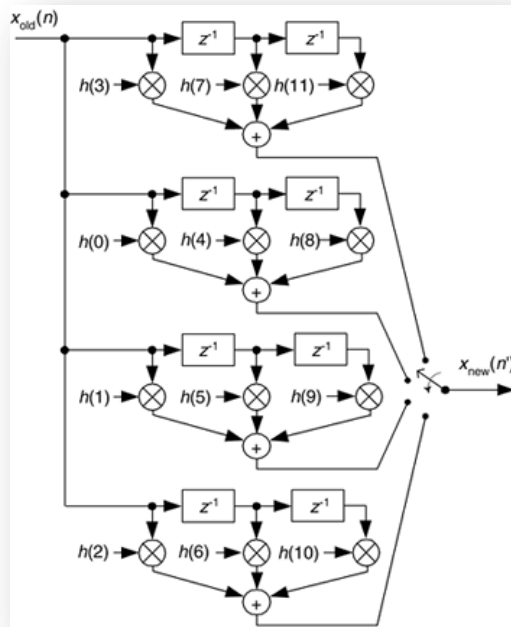
SOLUTIONS

-WRAP UP
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UPSAMPLER IMPLEMENTATION

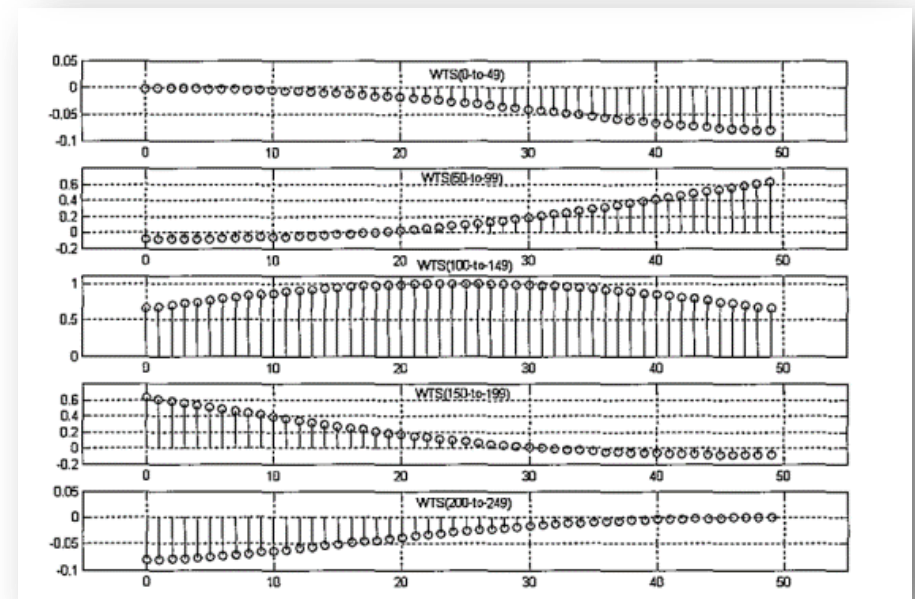
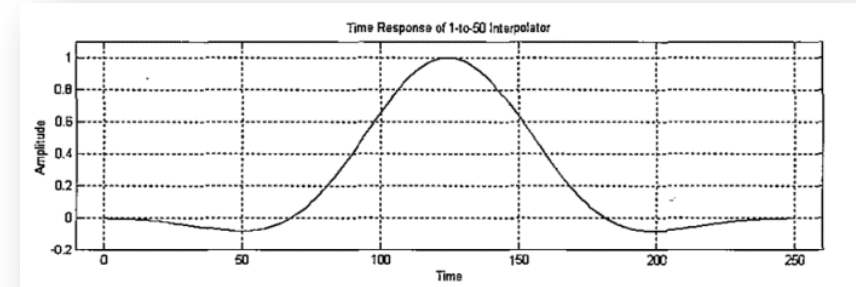
FARROW ARCHITECTURE

POLYPHASE DECOMPOSITION OF DELAY FILTER



Each branch provides a delayed sample by 1/P of the input sample interval

Equivalent to decompose the impulse response of the filter in segments mapped to the coefficient columns of the subfilters

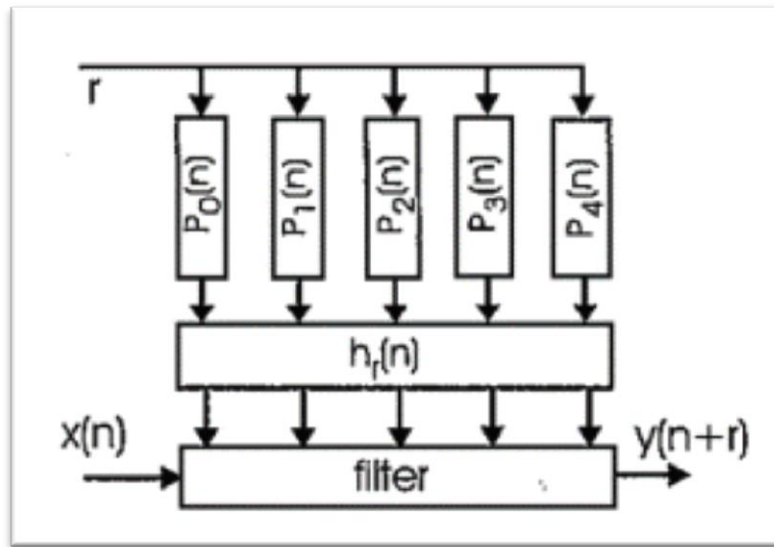


Original 250 tap filter split in 50 branches of 5 taps

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UPSAMPLER IMPLEMENTATION

APPROXIMATE THE SEGMENTS WITH A LOW ORDER POLYNOMIAL



- No need to store coefficient storage, only polynomials
- Evaluation of the polynomials at desired delay value gives coefficient, implicit interpolation of coefficient

With some further maths, it is possible to reorganize polynomials and the filter... We obtain a Taylor series representation of the desired output with the input and delay as only parameters

$$y(n + \Delta) = c_0(x) + c_1(x) \cdot \Delta + c_2(x) \cdot \Delta^2 + c_3(x) \cdot \Delta^3 + c_4(x) \cdot \Delta^4$$

-CONTEXT
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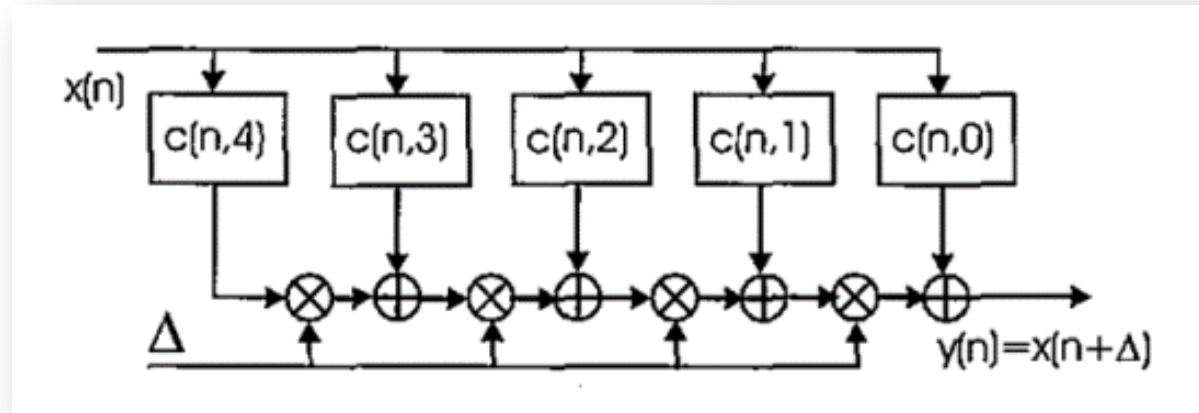
SOLUTIONS

-WRAP UP
-YOUR TIME...

UPSAMPLER IMPLEMENTATION

FINALLY, USE HORNER RULE TO EFFICIENTLY IMPLEMENT IT

$$y(\Delta) = c_0 + c_1\Delta + c_2\Delta^2 + c_3\Delta^3 + c_4\Delta^4$$
$$= c_0 + \Delta \cdot (c_1 + \Delta \cdot (c_2 + \Delta \cdot (c_3 + \Delta \cdot c_4)))$$



Farrow architecture

- CONTEXT
- MOTIVATION
- BACKGROUND
- OBJECTIVE

SOLUTIONS

- WRAP UP
- YOUR TIME...

UPSAMPLER IMPLEMENTATION

VARIABLE FRACTIONAL DELAY & CONTROL LOGIC TO COMPUTE DELAY

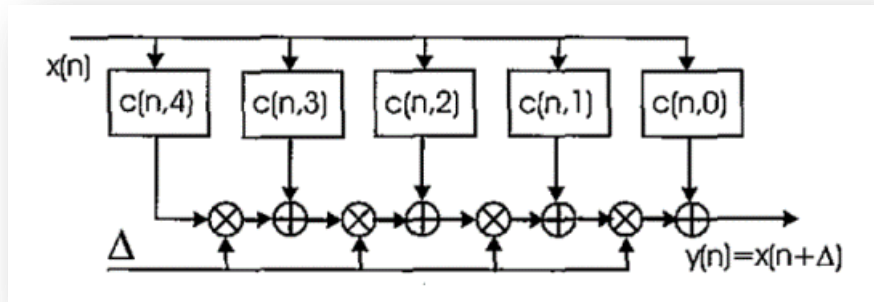
-CONTEXT
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SOLUTIONS

-WRAP UP
-YOUR TIME...

FARROW ARCHITECTURE

- Polyphase decomposition of reconstruction shifted filter (static)
- Coefficients approximated by polynomials
- Reshuffle polynomials and filter architecture to obtain a Taylor series representation of the desired output



PARAMETERS; input and delay

PHASE ACCUMULATORS

- Delay is the difference between two counters, phase accumulators
- One running at input sampling rate
- Second running at output sampling rate
- Real time computation of the delay for arbitrary sampling rate conversion

