

# Introducing Fixed Frequency Clock Operation on the CERN VXS LLRF Platform

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# Outline

- Context
- Original Sweeping Clock LLRF Implementation
- Motivation for Change
- Requirements for a Fixed Frequency Clock Scheme
- FTW Distribution / Synchronisation
- Why Clock at 122.7 MHz ?
- Fixed Frequency Clock LLRF implementation
  - RF Receiver (DDC)
  - RF Modulator (SDDS)
- Results
- References
- Conclusion

# Context

## Two families of synchrotrons at CERN

1. VXS [1] based LLRF systems [2] with narrow-band (multi-harmonic) feedback
  - a) Typically smaller circular accelerators / decelerators:
    - PSB Proton Synchrotron Booster (4 rings)
    - LEIR Low Energy Ion Ring
    - ELENA Extra Low ENergy Antiproton decelerator
    - AD P-bar decelerator
  - b) Single  $f_{\text{rev}}$  side-bands treated individually
  - c) Large RF frequency sweep range (ELENA ~factor 7)
  - d) All of which are / will use **Finemet cavities**

VXS LLRF of these machines are the topic of **this talk**, see also:

- *P-91 CERN's VXS LLRF platform: new features & beam results*  
*Maria Elena Angoletta, CERN, Geneva, Switzerland*

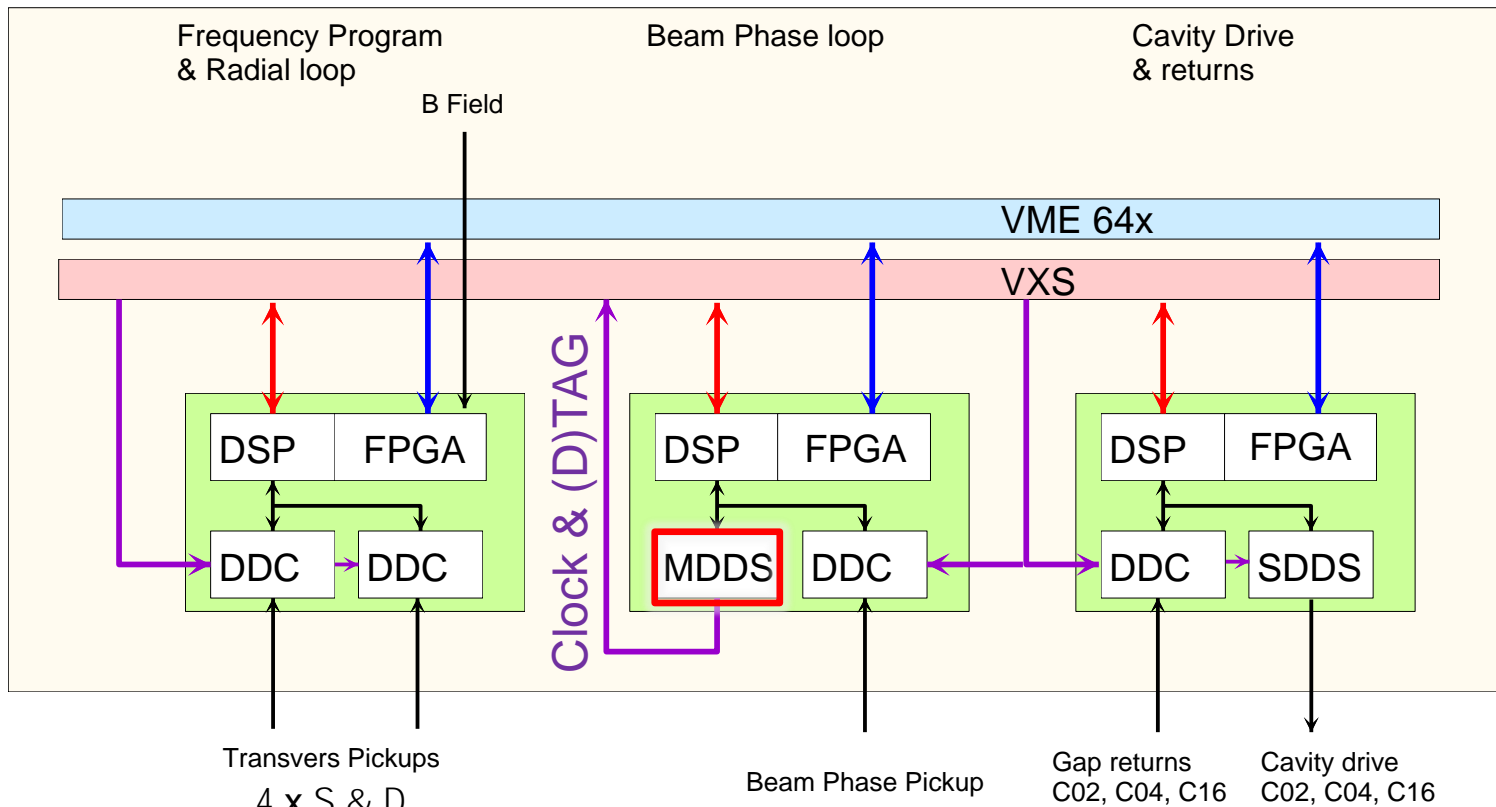
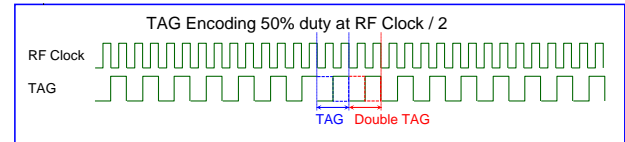
2. LLRF systems with wide-band (many  $f_{\text{rev}}$  side-bands) feedback
  - SPS Super Proton Synchrotron
  - LHC Large Hadron Collider

These machines are the topic of:

- *O-24: Beam Synchronous Processing: Fixed Clock and RF Regeneration. New Paradigms for CERN SPS LLRF*  
*Javier Galindo Guarch, CERN, Switzerland*
- *P-77 Implementation of a One-Turn Delay Feedback with a Fractional Delay Filter*  
*Lorenz Schmid, Philippe Baudrenghien, Gregoire Hagmann, CERN, Geneva, Switzerland*
- *P-92 The SPS LLRF upgrade project: An update*  
*Gregoire Hagmann<sup>1</sup>, Javier Galindo Guarch<sup>1,2</sup>, Gerd Kotzian<sup>1</sup>, Lorenz Schmid<sup>1</sup>, Arthur Spierer<sup>1</sup>, Philippe Baudrenghien<sup>1</sup>, <sup>1</sup>CERN, Geneva, Switzerland, <sup>2</sup>UPC, Barcelona, Spain*

# Original Sweeping Clock LLRF Implementation (1)

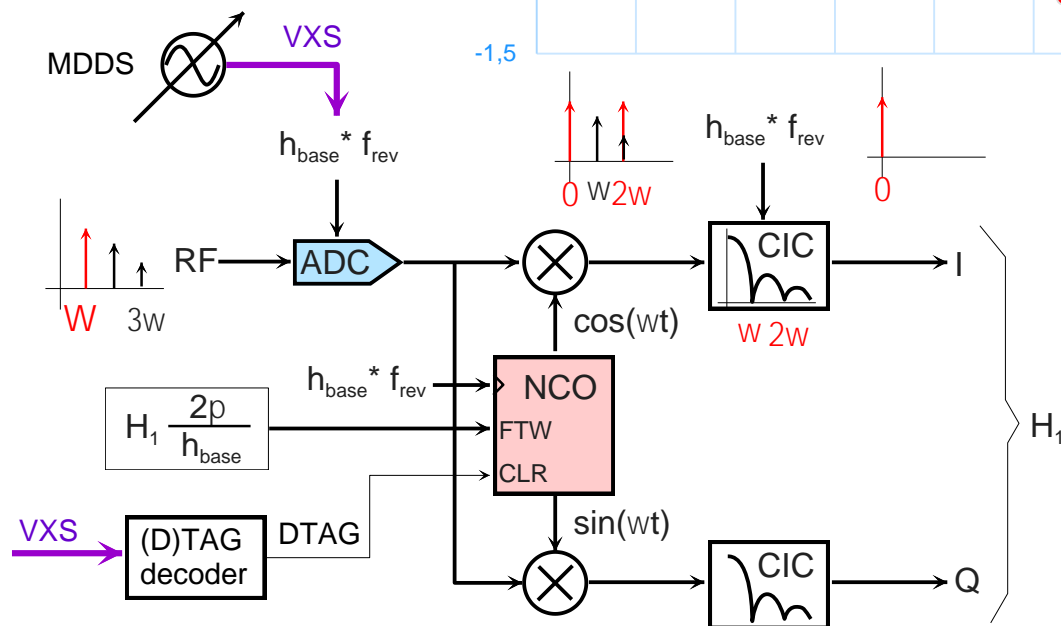
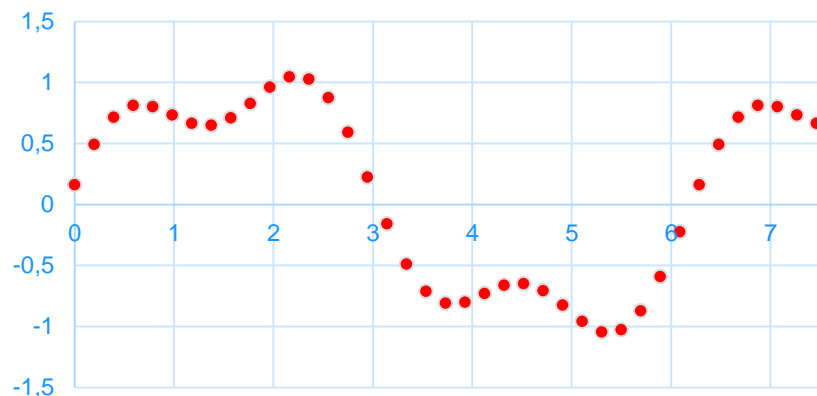
- Common Master DDS generated (RF) clock  $f_{rev} * h_{base}$  (~40 – 125 MHz)
  - Frequency Tuning Word controlled by one DSP
  - Distributed via a dedicated VXS channel to all modules
- Common Master DDS firmware generated TAG / DTAG
  - Revolution frequency clock +
  - Local Oscillator Synchronisation events
  - Distributed via a dedicated VXS channel to all modules



# Original Sweeping Clock LLRF Implementation (2)

- Typical RF receiver DDC

Sampled RF for  $h_{\text{base}} = 32$

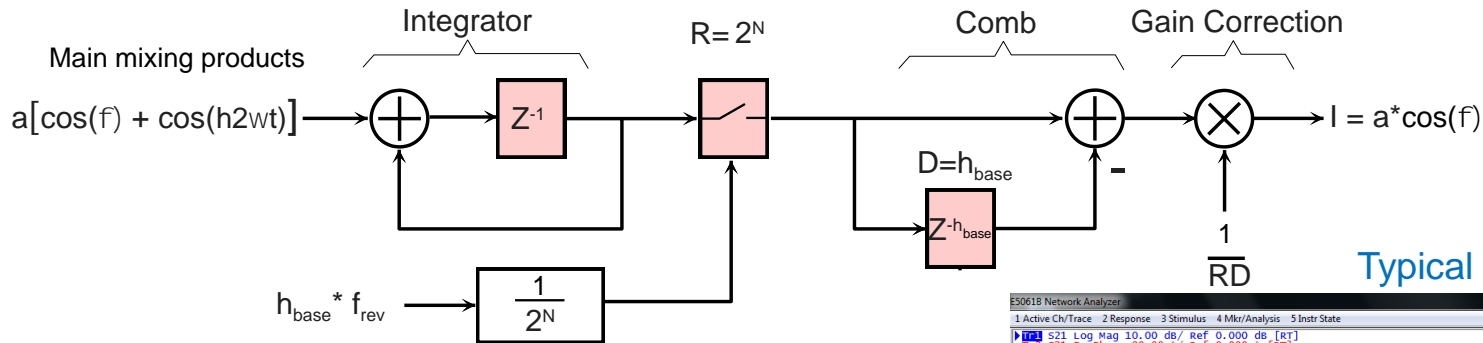


# Original Sweeping Clock LLRF Implementation (3)

## CIC Filter

- NULLs automatically track “ $f_{rev}$  multiples”
- Gain Correction => simple bit shift ( $h_{base}$  = power of 2)
- Linear Phase

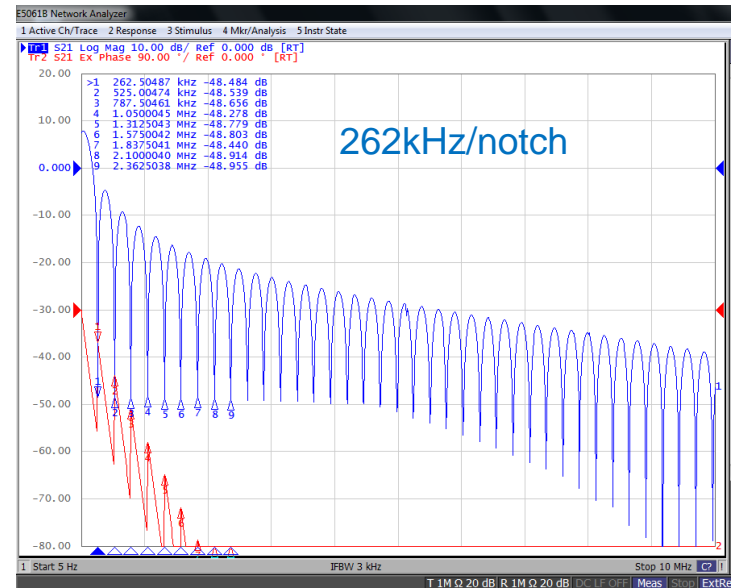
$$Z^{-1} = \frac{1}{h_{base} * f_{rev}}$$



Typical Response

0dB

-50dB

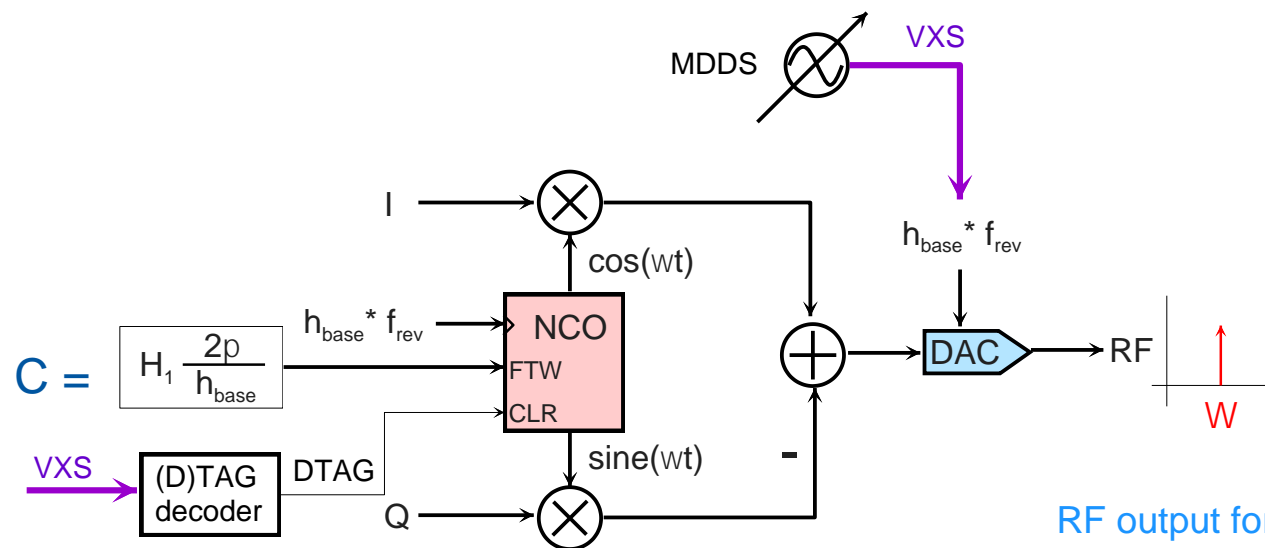


CIC Naming conventions, R, D, according to [3]

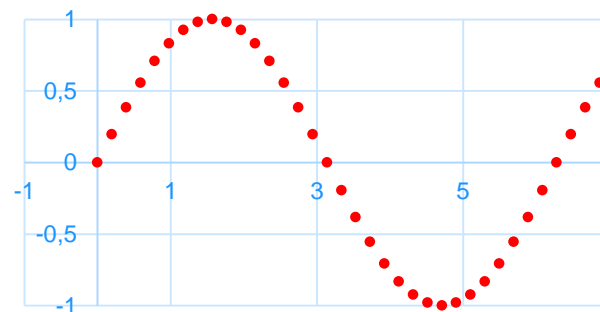


# Original Sweeping Clock LLRF Implementation (4)

- Typical RF vector modulator SDDS
  - I/Q in base-band (from DSP) are up-modulated to RF
  - Sample spacing =  $f(f_{rev}) = T_{rev} / h_{base}$



RF output for  $h_{base} = 32$





# Motivation for Change

## Issues with sweeping clock

- MDDS clock constraint:  $f_{\min} \text{ VXS } (\sim 20\text{MHz}) \leq f_{\text{MDDS}} \leq f_{\max} \text{ ADC } (125 \text{ MHz})$ 
  - Limited sweep range
  - Puts constraints on  $h_{\text{base}}$  (granularity)
  - DDC ADC anti-aliasing LPF cut-off frequency ?
  - SDDS DAC reconstruction LPF cut-off frequency ?
- Operate ADC well below optimal frequency
- Coherent sampling:
  - Folds back harmonic distortion onto signal
  - Oversampling ENOB gain reduced (noise  $\neq$  white & uniform)
- Tagging unreliable at certain frequencies due to FPGA path delays

## **Sweeping Clock System**

## Properties with fixed frequency clock

- MDDS clock frequency fixed
  - Nearly unlimited frequency range for DDC / SDDS
  - Sample granularity always maximal
  - DDC ADC anti-aliasing LPF fixed
  - SDDS DAC reconstruction LPF fixed
- ADC operated at optimal frequency
- Incommensurate sampling:
  - Harmonic distortion mostly out of band
  - Maximize oversampling ENOB gain
- Tagging can easily be made reliable

## **Fixed Frequency Clock System**

# Requirements for a Fixed Frequency Clock scheme

1. Reliable Frequency Tuning word (FTW) distribution
  - a) Must maintain absolute synchronism (avoid phase slippage) between system-wide distributed NCOs
2. Capability to deliver clock / FTW signals to external systems (over fibre)
  - a) Frequency > lower limit media (ac coupling)
  - b) DC balanced
3. A suitable harmonic (mixing by-products) suppression filter for the DDC demodulators
4. Modest complexity to allow implementing multi-demodulator / demodulator banks. One channel per required harmonic.

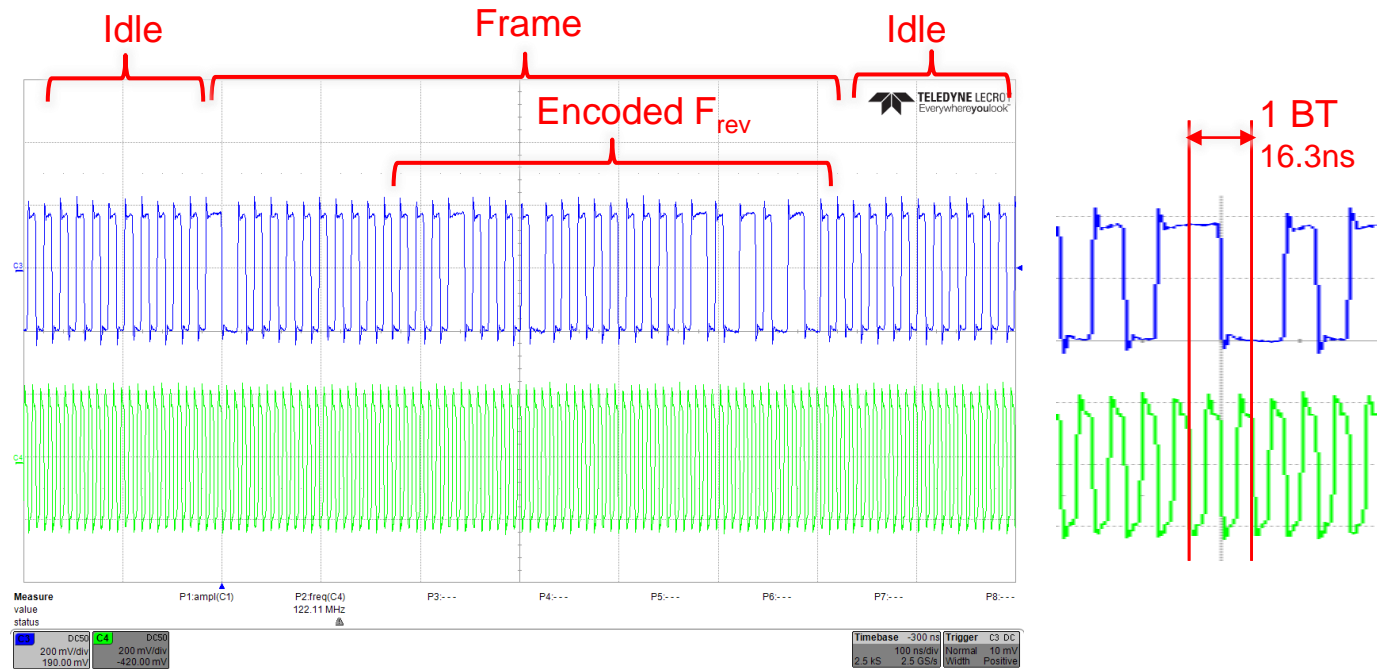
# FTW Distribution / Synchronisation

## Finally retained solution:

1. Multicast the fixed MDDS clock on the VXS
2. Use the MDDS clock synchronous TAG-line to VXS multicast:
  - a) Manchester Encoded (DC-balanced)  $F_{rev}$  value [Hz]
  - b) Optional Double TAG, phase accumulator reset
  - c) Transmission once per DSP cycle  $10\mu\text{s}$  typical
  - d) Received by all nodes at the exact same clock
3. Multi-casted clock and TAG routable to SFP optical interfaces

TAG-line

MDDS clock  
122.7 MHz



# Why Clock at 122.7 MHz ?

To convert the distributed numerical  $f_{rev}$  [Hz] value to FTW we need M:

$$M = \frac{FTW}{f_{rev}}$$

From:

*MDDS equation:*

$$f_{rev} = \frac{FTW}{2^{32}} f_{MDDS}$$

and

Maximal ADC (MDDS) frequency = 125 MHz

we get:

$$M = \frac{FTW}{f_{rev}} = \frac{2^{32}}{125 * 10^6} = 34.36 \dots$$

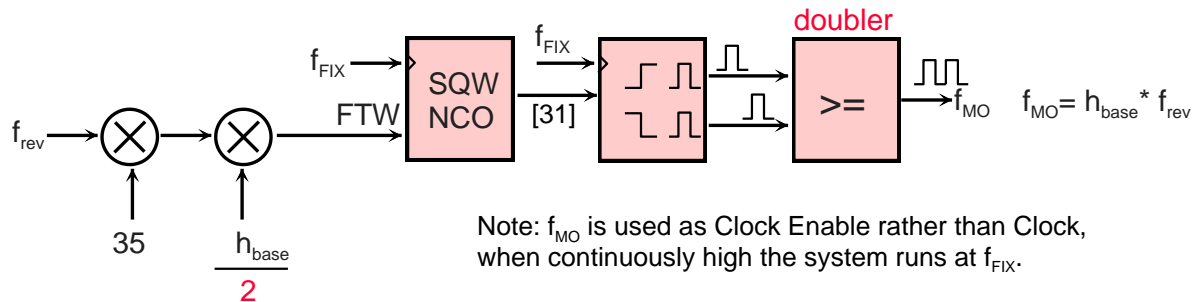
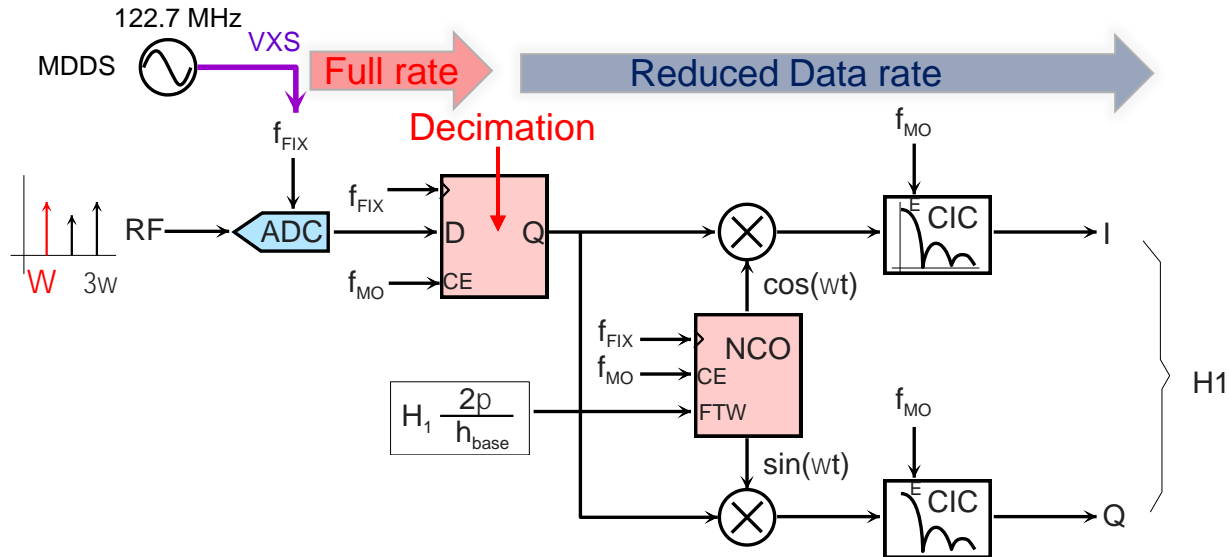
Rounding M up to the nearest integer **35** we get:

$$f_{MDDS} = f_{FIX} = \frac{2^{32}}{35} = 122.713.351,314 [Hz]$$

# Fixed Frequency Clock LLRF Implementation (1)

## RF Receiver, 1<sup>st</sup> idea:

- Clock all elements with  $f_{\text{FIX}}$  and Clock Enable  $f_{\text{MO}}$
- Tune CIC filter notches to  $f_{\text{rev}}$  harmonics using Clock Enable  $f_{\text{MO}}$
- A shame to throw away most ADC samples...

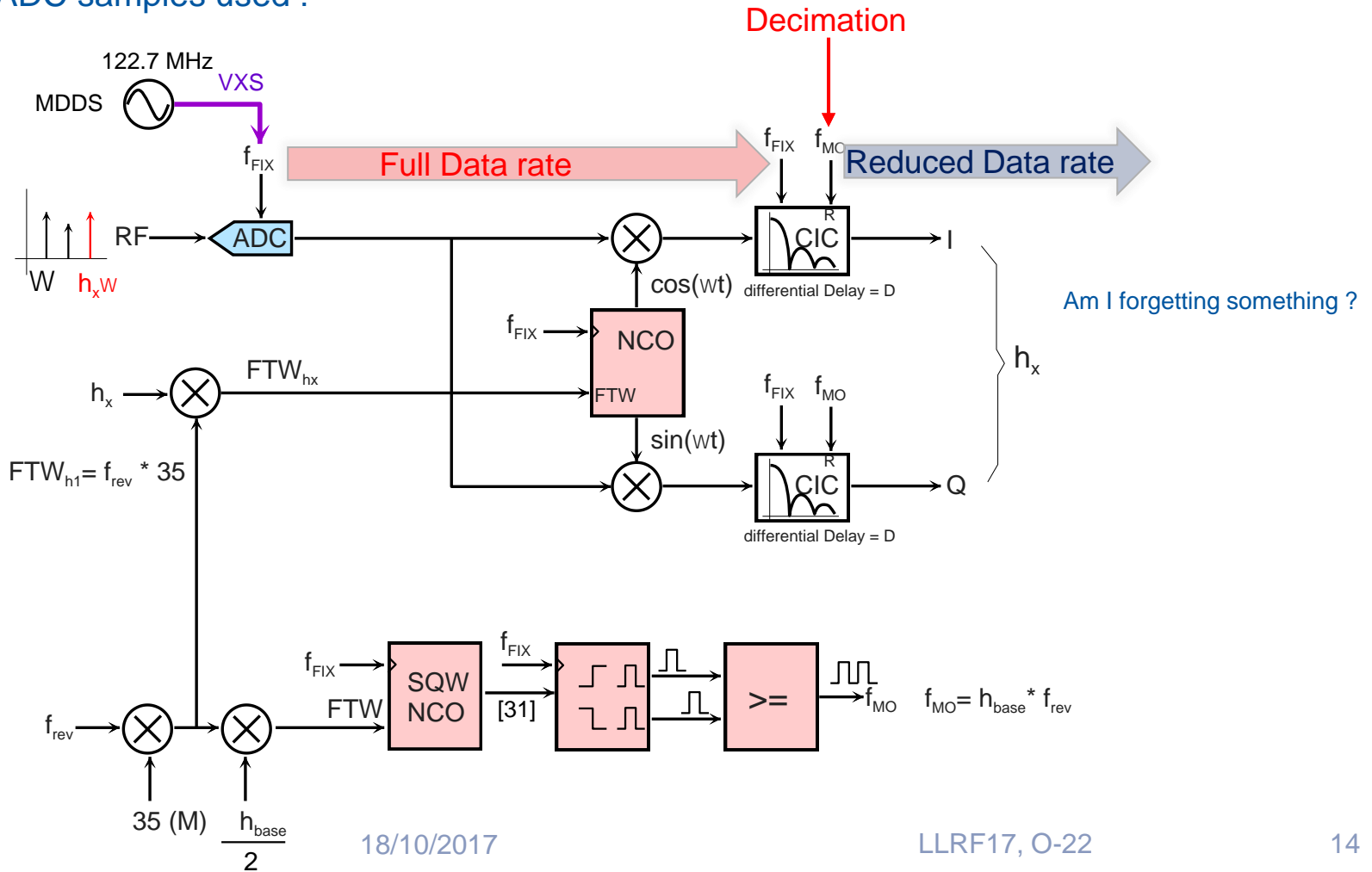


Note:  $f_{\text{MO}}$  is used as Clock Enable rather than Clock, when continuously high the system runs at  $f_{\text{FIX}}$ .

# Fixed Frequency Clock LLRF Implementation (2)

## RF Receiver, 2<sup>nd</sup> idea:

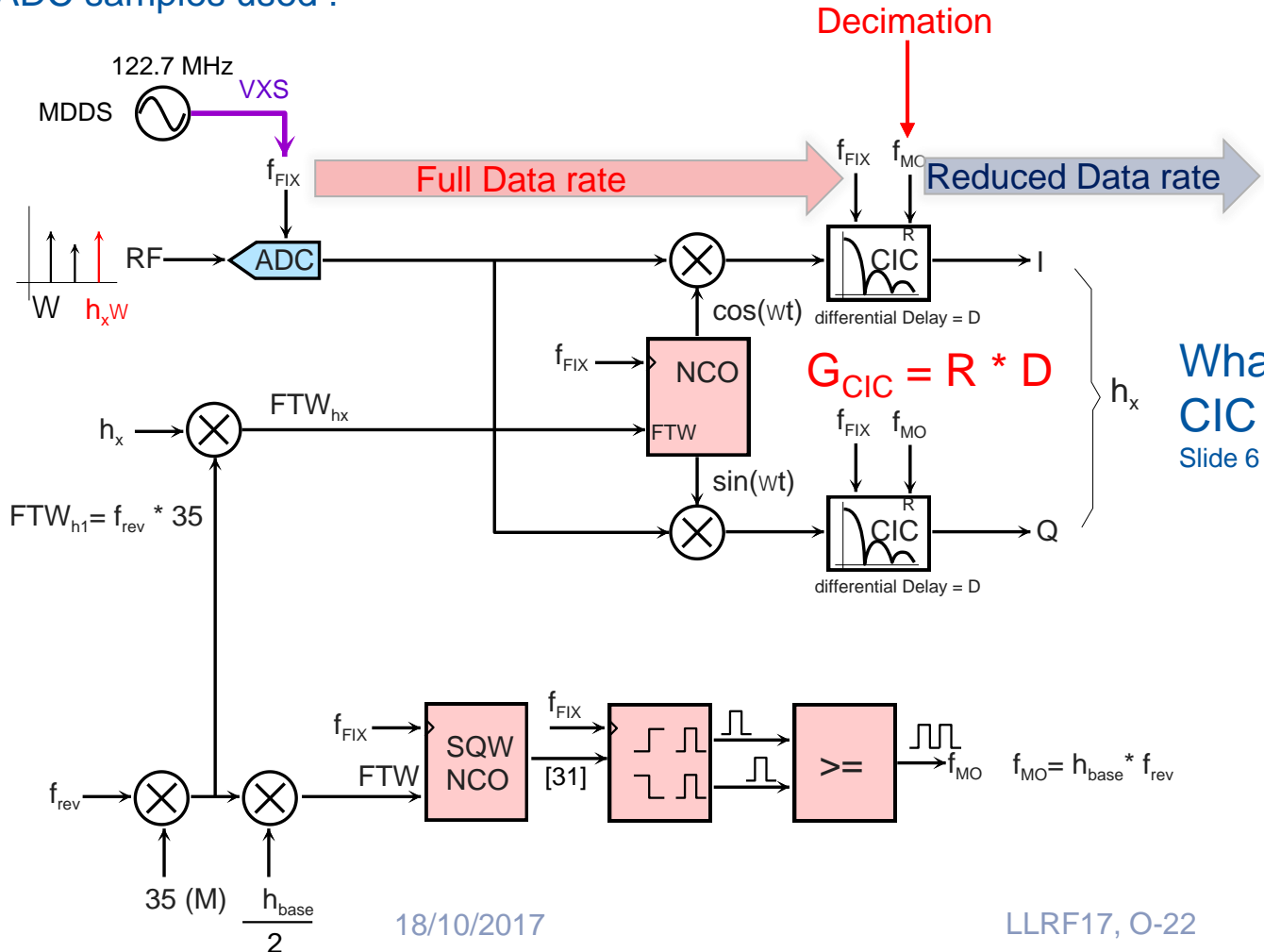
- Clock all elements, including CIC integrator with  $f_{\text{FIX}}$
- Tune CIC filter notches (comb) to  $f_{\text{rev}}$  harmonics using Clock Enable  $f_{\text{MO}}$
- Now need to tune NCO FTW
- All ADC samples used !



# Fixed Frequency Clock LLRF Implementation (3)

## RF Receiver, 2<sup>nd</sup> idea:

- Clock all elements, including CIC integrator with  $f_{\text{FIX}}$
- Tune CIC filter notches (comb) to  $f_{\text{rev}}$  harmonics using Clock Enable  $f_{\text{MO}}$
- Now need to tune NCO FTW
- All ADC samples used !



What about the  
CIC filter gain !?  
Slide 6

# Fixed Frequency Clock LLRF Implementation (4)

CIC Gain Compensation:

$$G_{CIC} = RD(f_{rev}) = \frac{f_{FIX}}{f_{MO}} D = \frac{\overbrace{f_{FIX}}^R}{\cancel{h_{base}} * f_{rev}} \overbrace{2^N h_{base}}^D$$

N = Differential delay shift control (0=notch at  $f_{rev}$ )

From slide 10 we have:

$$f_{FIX} = \frac{2^{32}}{M} = \frac{2^{32}}{35}$$

And finally the required compensation gain:

$$G_{comp}(f_{rev}) = \frac{1}{G_{CIC}} = \frac{f_{rev}M}{2^{32+N}}$$

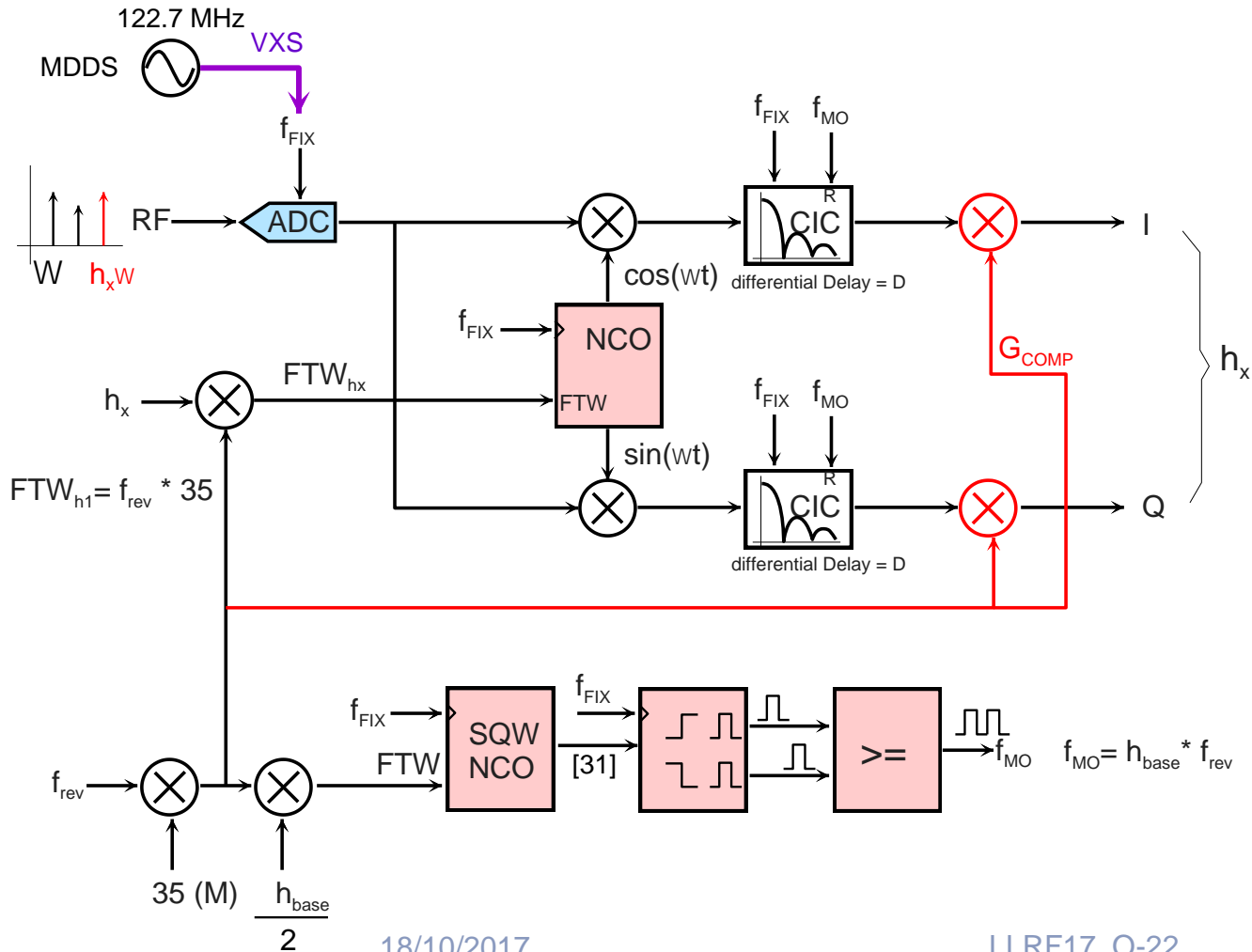
- Simply proportional with  $f_{rev}$  (as expected)
- Exactly equals the normalised FTW for harmonic 1 !



# Fixed Frequency Clock LLRF Implementation (5)

## RF Receiver, trial 2<sup>nd</sup> idea:

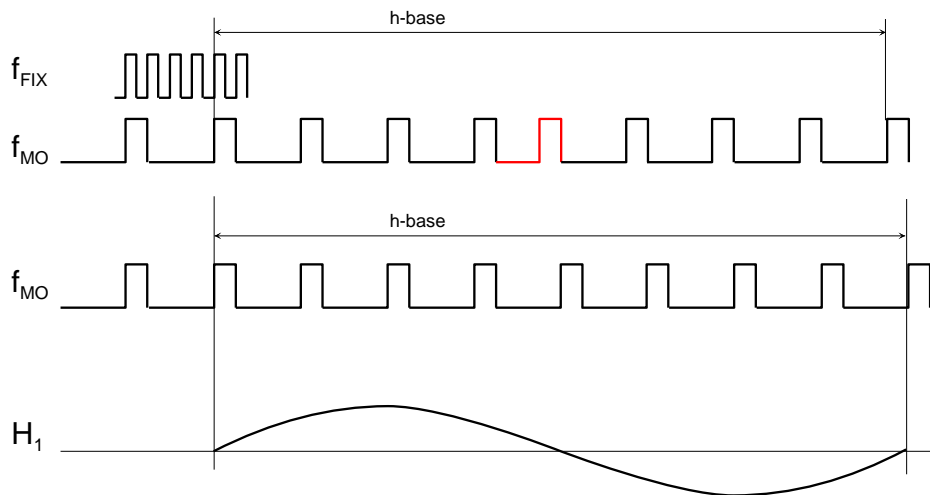
- Added CIC Gain correction
- **Behind** the CIC to keep full precision (at the cost of a DSP48E)



# Fixed Frequency Clock LLRF Implementation (6)

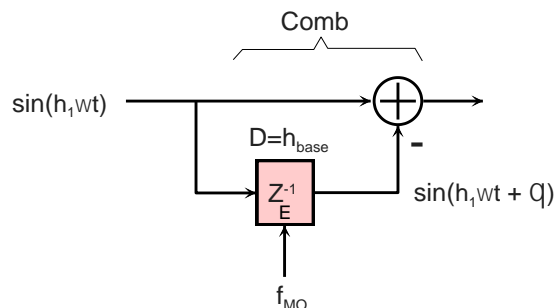
## CIC Comb filter temporal quantisation effects:

- $F_{MO}$  pulses follow the average  $f_{rev} * h_{base}$  but will jitter by  $T_{FIX}$



The CIC Comb filter uses destructive interference to suppress unwanted harmonics

- With the  $f_{MO}$  jitter the direct and delayed harmonics will not perfectly cancel



$$\theta = 2\pi \frac{T_{FIX}}{T_{rev}} = 2\pi \frac{f_{rev}}{f_{FIX}} [\text{rad}]$$

*Worst-case phase error on a sample*

# Fixed Frequency Clock LLRF Implementation (7)

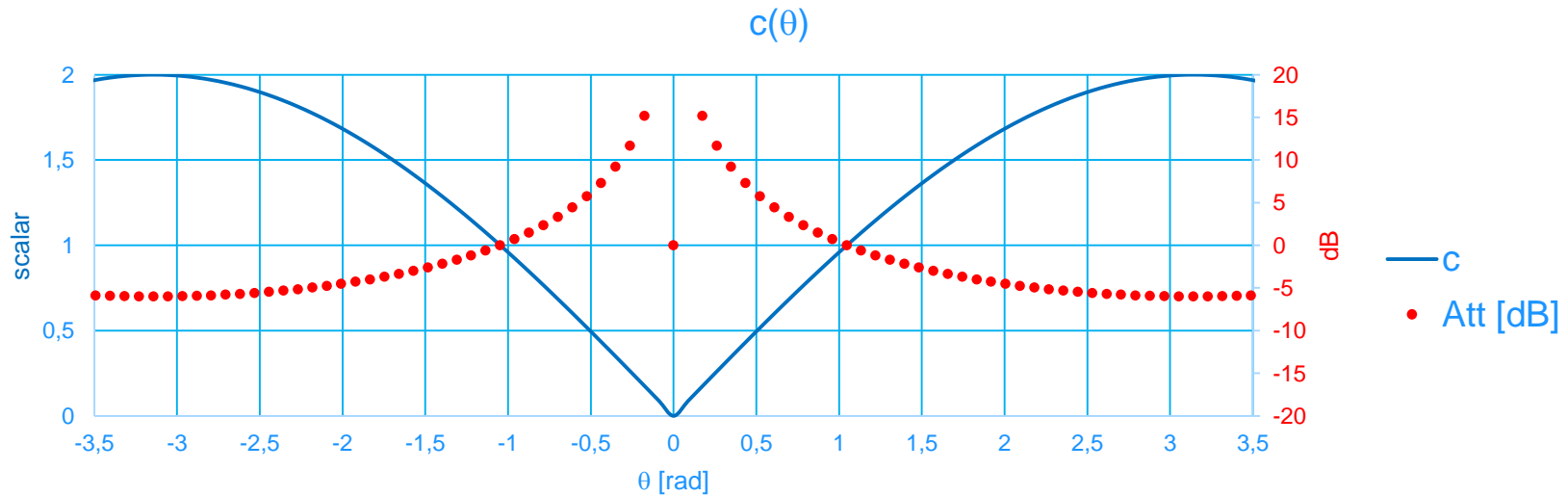
## CIC Comb filter temporal quantisation effects:

Considering the difference of sine wave we can write the following general equation:

$$\sin(x) - \sin(x + \theta) = c * \sin(x + \varphi)$$

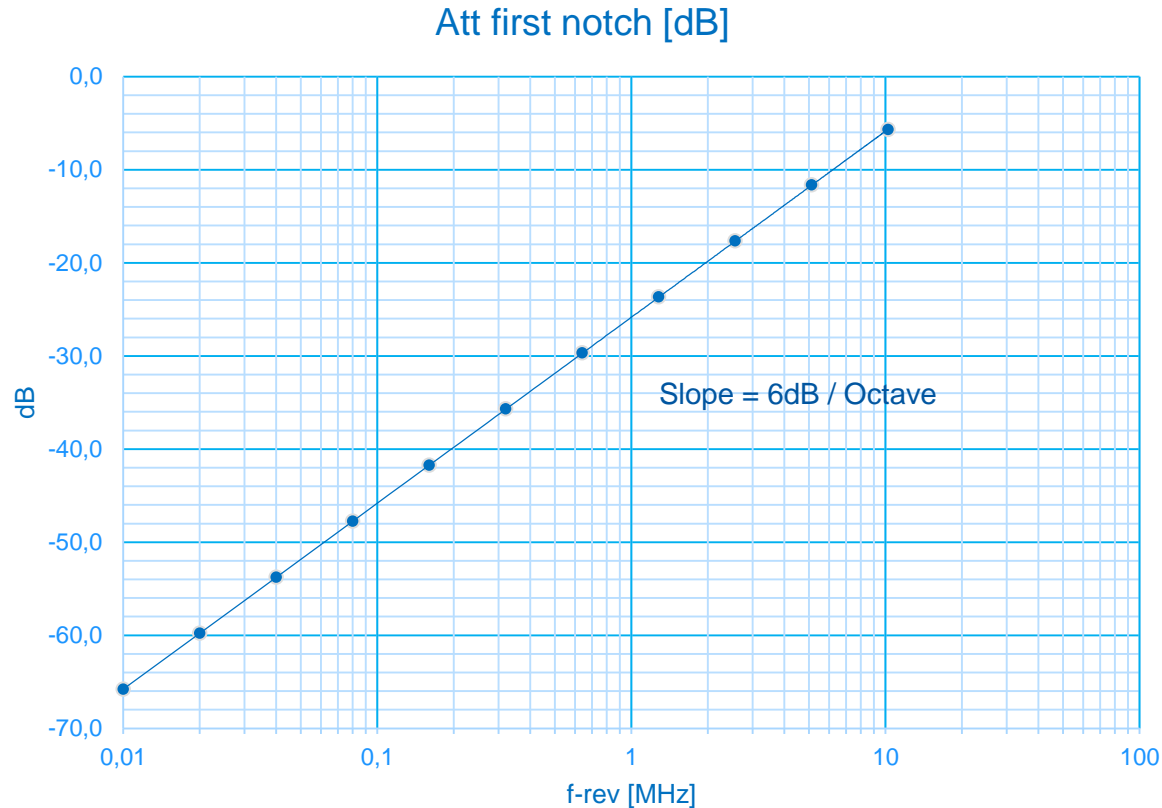
Magnitude harmonic leakage at the CIC filter output  $\propto c$

$$c(\theta) = \sqrt{2 + 2 \cos(\pi - \theta)} = 2 \left| \sin\left(\frac{\theta}{2}\right) \right|$$



# Fixed Frequency Clock LLRF Implementation (8)

## CIC Comb filter temporal quantisation effects:

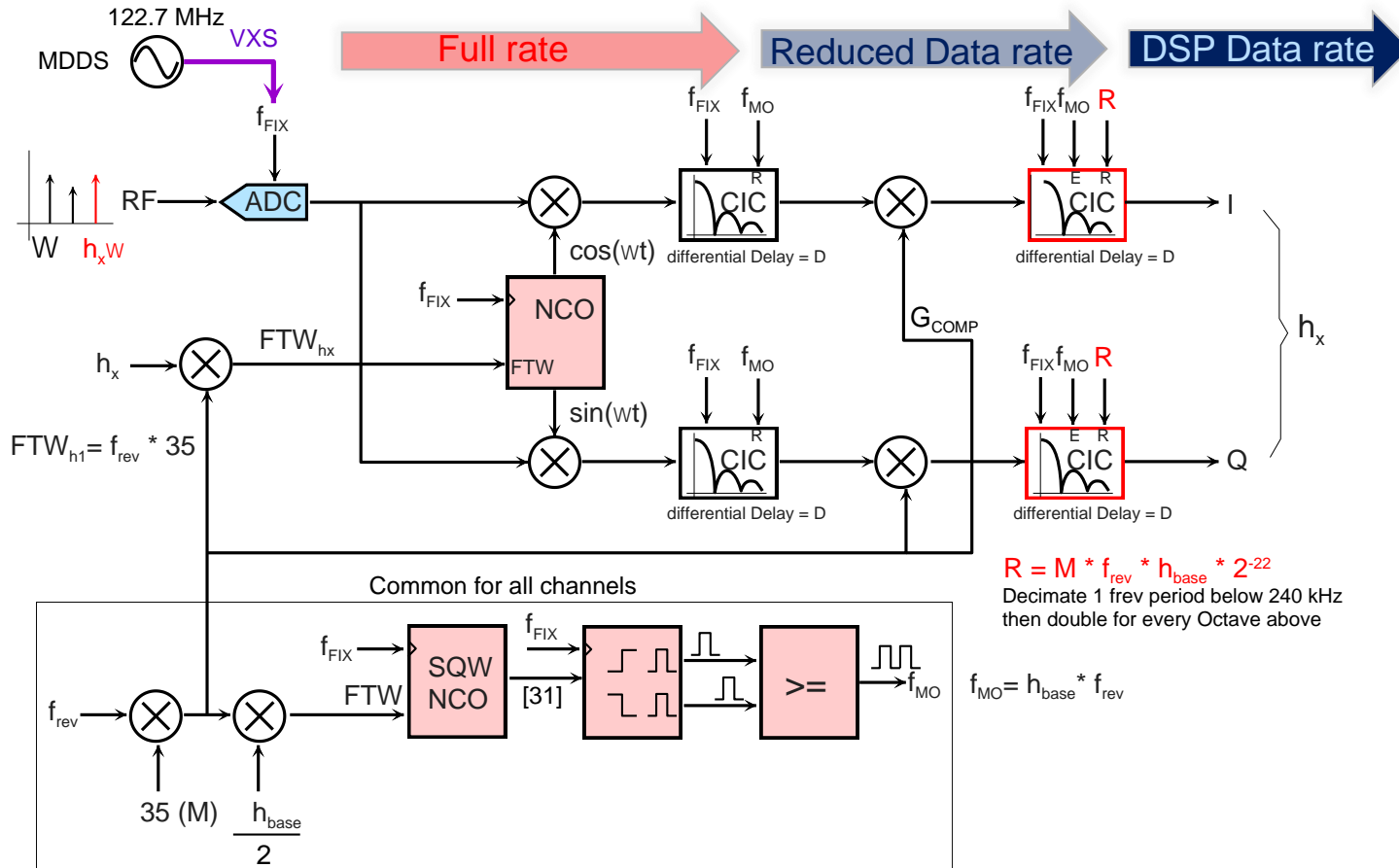


Plot of the attenuation of the first  $f_{rev}$  harmonic as function of  $f_{rev}$

Note: Additional attenuation (6dB / Octave) due to 1<sup>st</sup> order integrator (CIC input) not accounted for  
Overall harmonics attenuation expected to be independent of the frequency.

# Fixed Frequency Clock LLRF Implementation (9)

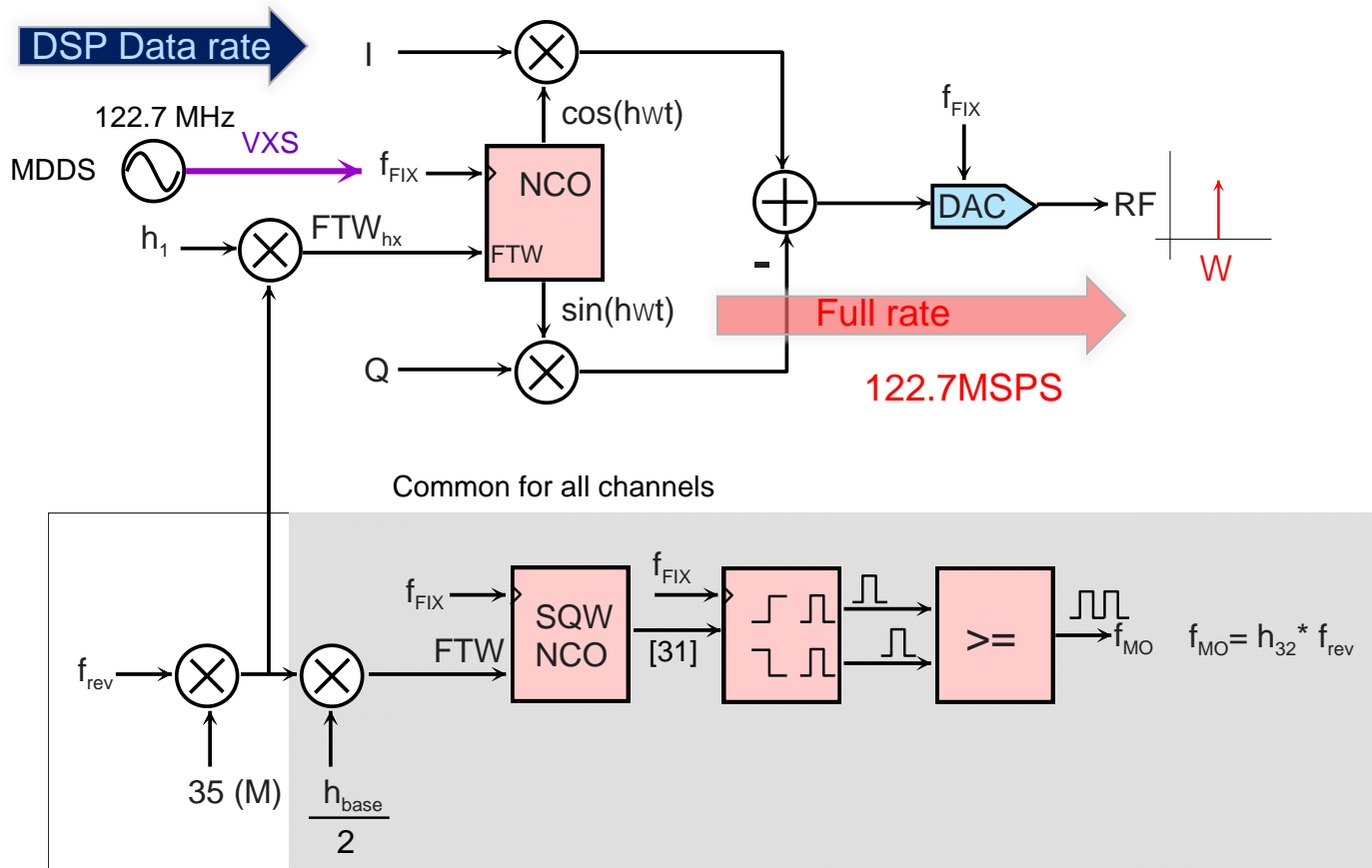
## Final Receiver:



Note: A Post Filter (averaging) has been added to reduce the data rate to near that of the DSP.

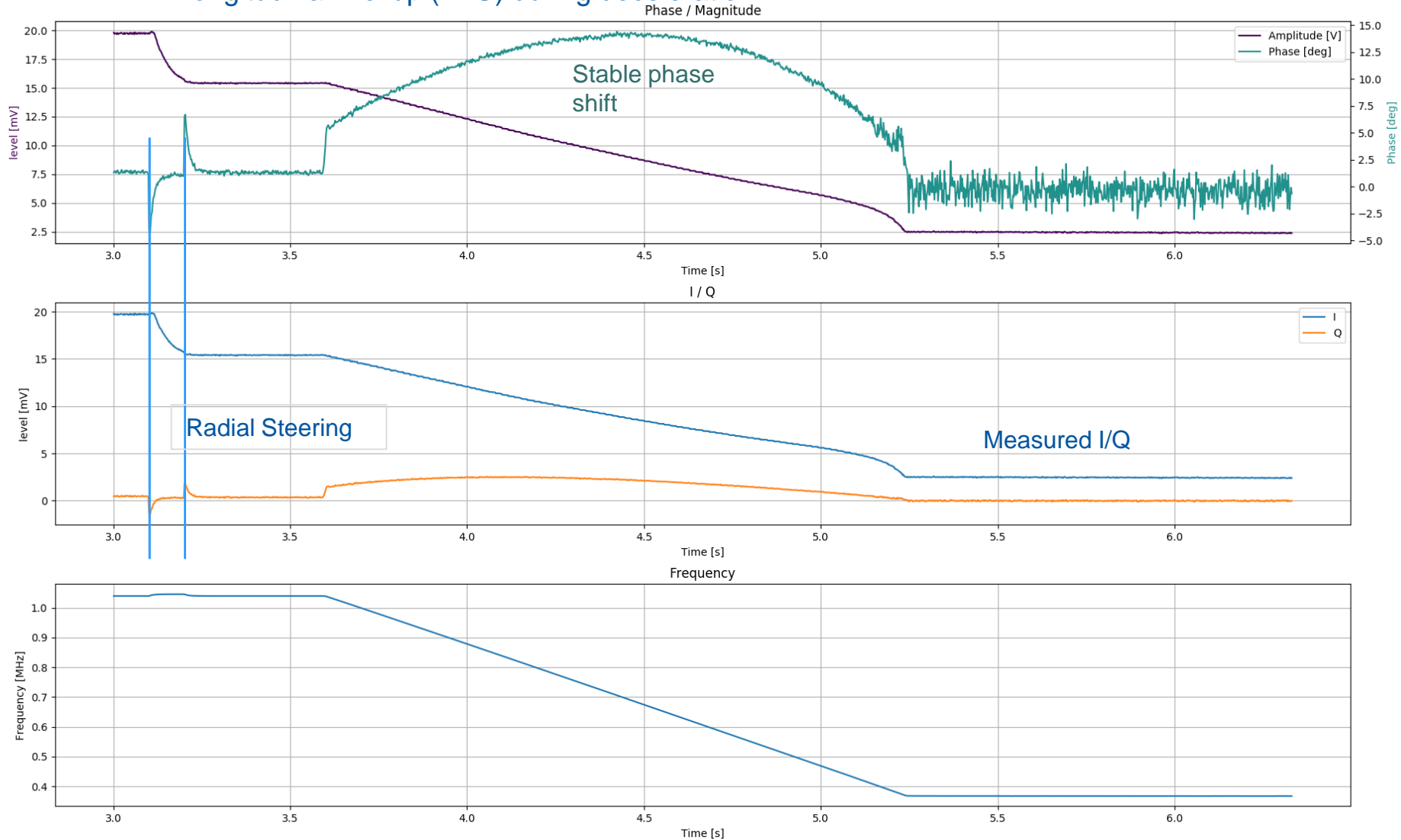
# Fixed Frequency Clock LLRF Implementation (10)

## Final Modulator:



# Results (1)

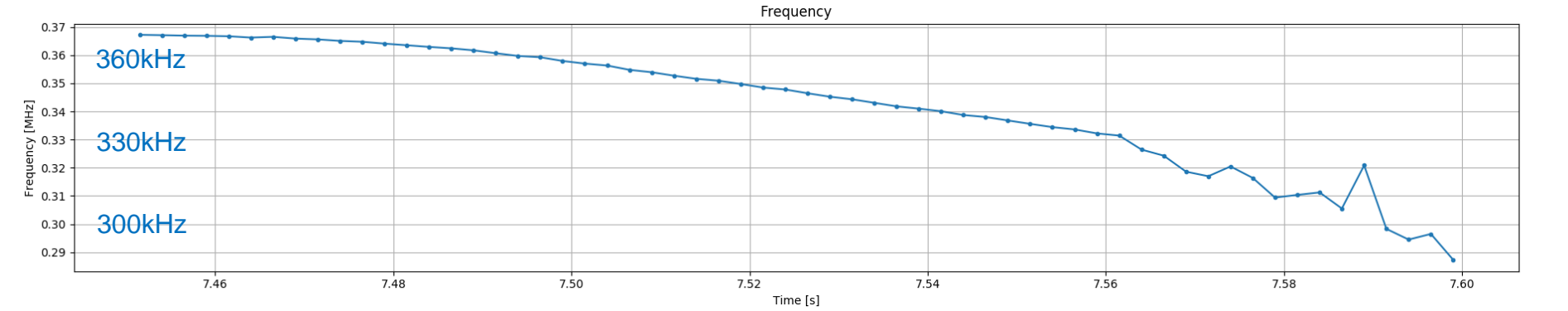
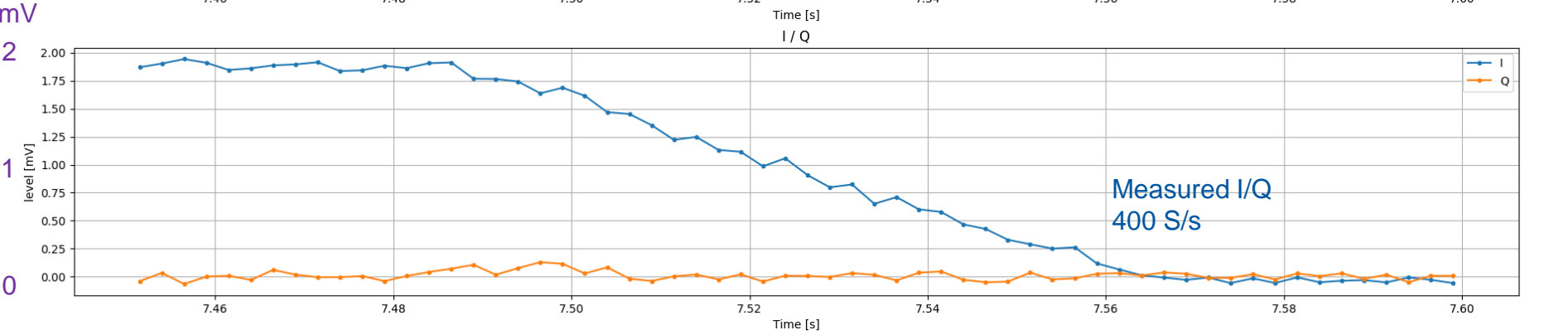
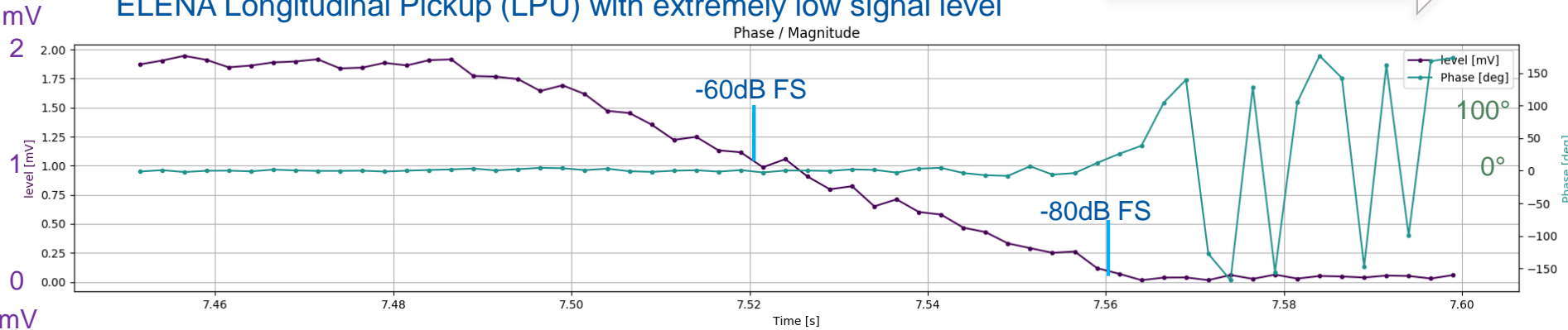
## ELENA Longitudinal Pickup (LPU) during deceleration



# Results (2)

## ELENA Longitudinal Pickup (LPU) with extremely low signal level

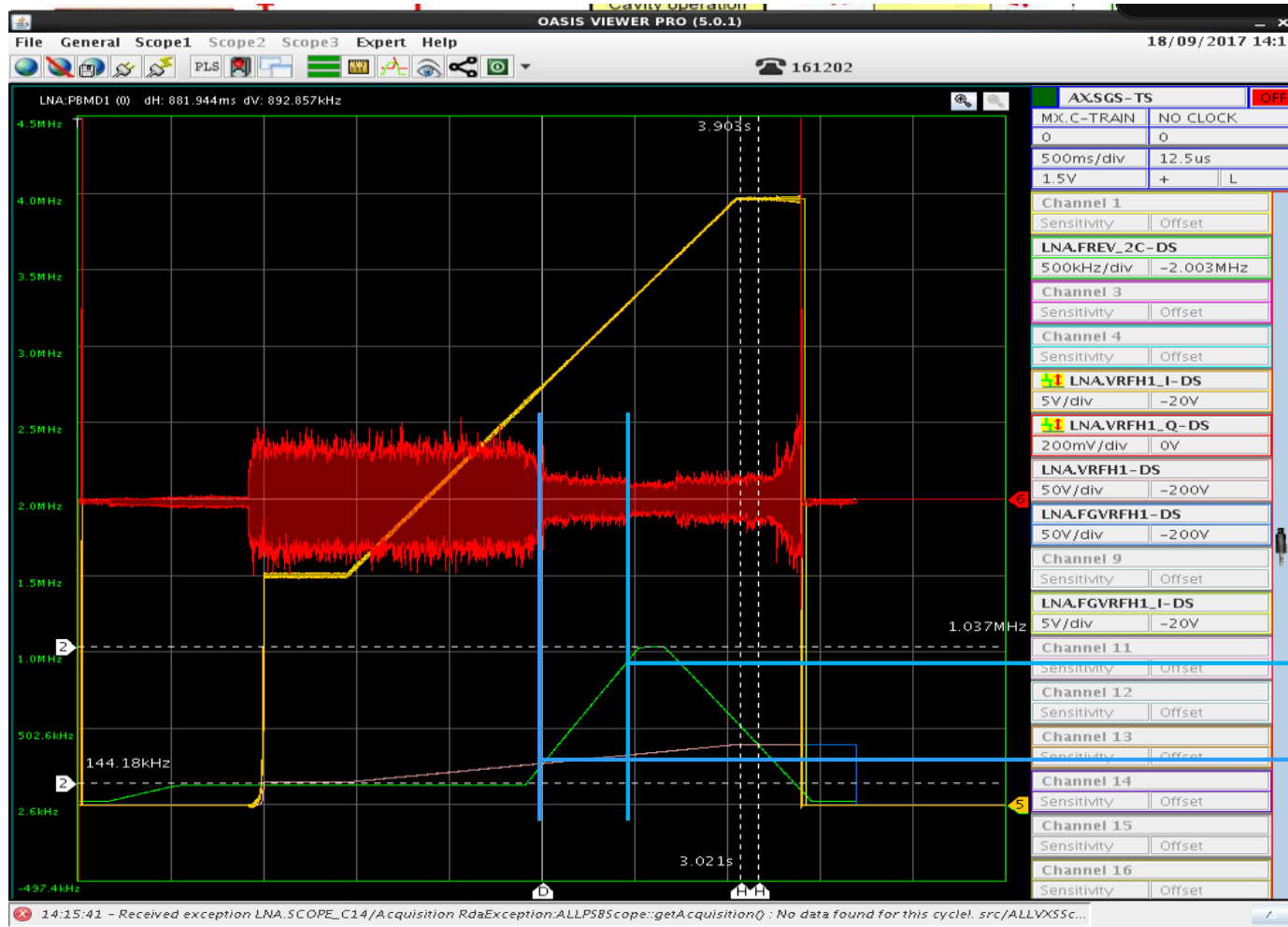
Beam Signal Lost





# Results (3)

VGAP (H2) Measurement: Post Filter noise reduction  $f_{rev} > 240\text{kHz}$



# References

- [1] ANSI / VITA 41.0, “VXS VMEbus Switched Serial Standard” (<http://www.vita.com/vxs.html>).
- [2] LLRF 2013 Lake Tahoe: A Leading-edge Hardware Family for LLRF and Diagnostics applications in CERN’s Synchrotrons, J. Molendijk et al.
- [3] Digital Signal Processing with Field Programmable Gate Arrays U. Meyer-Baese
- [4] LLRF 2015 Digital Receiver and Modulator Architecture for Multi-harmonic RF Finemet Operation, J. Molendijk

# Conclusion

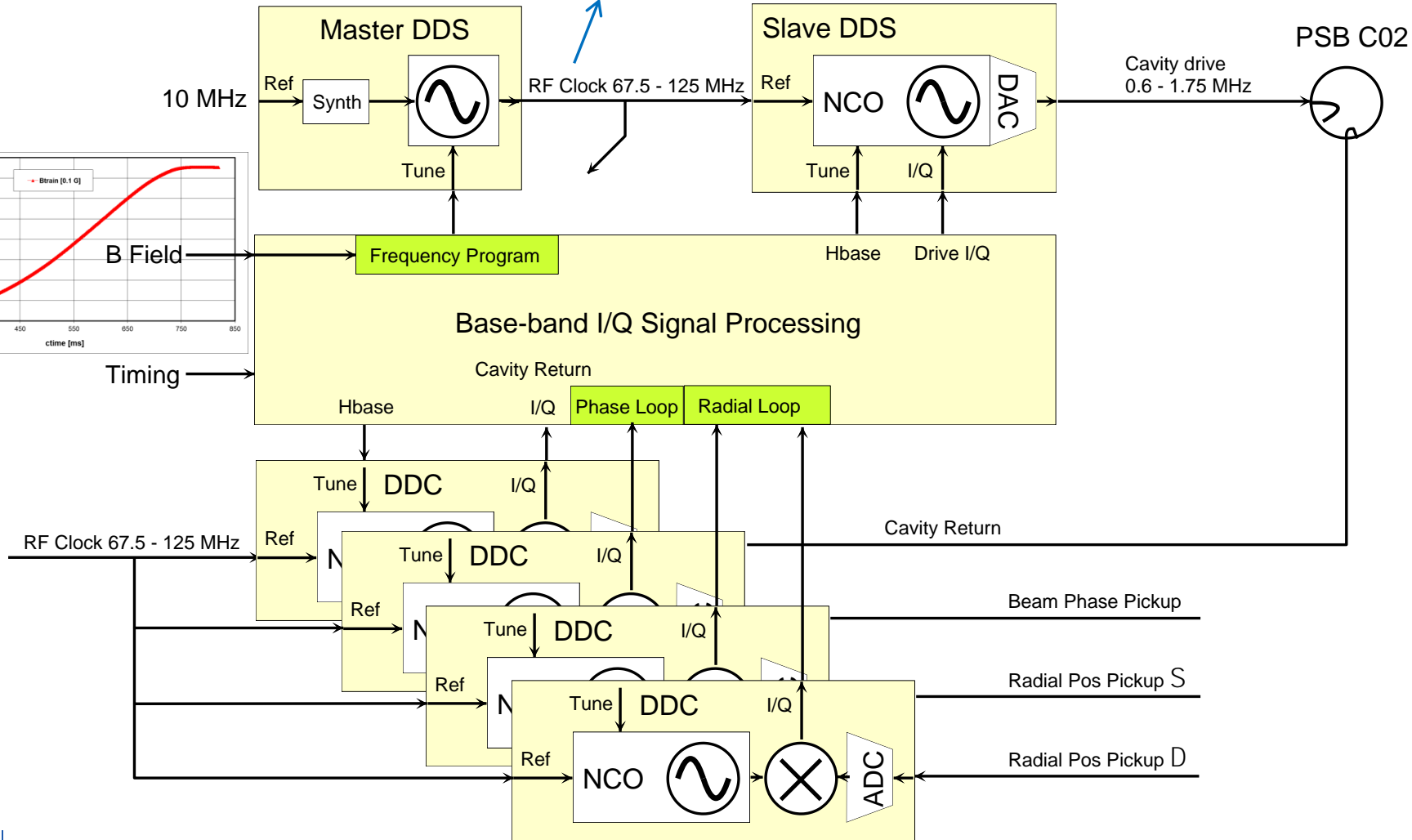
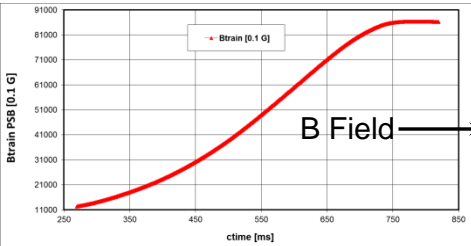
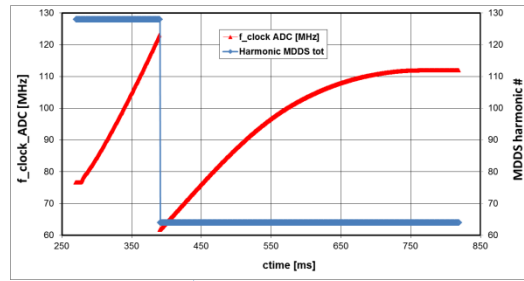
## Fixed Frequency operated VXS LLRF

- Successful operation (ELENA commissioning) since early this year
- Further tests using CERN PSB test-crate connected to ring 4 foreseen 2018
  - + Add (8/16 Channel) Multi-harmonic [4] implementation
- Deployment to all small machines (PSB\*, LEIR, AD\*) during the long shutdown (LS2) starting 2019

\* To be equipped with Finemet cavities during LS2

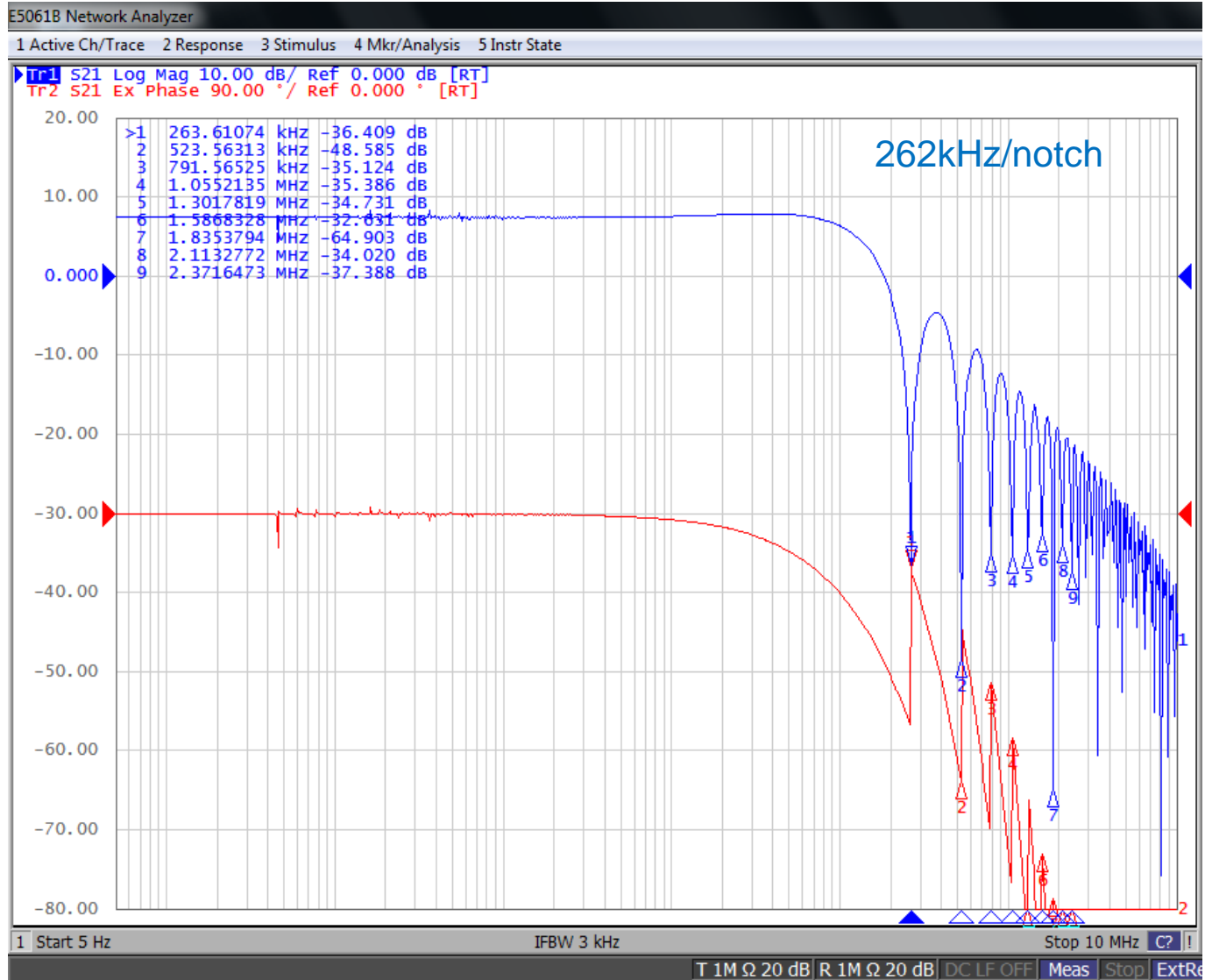
# Backup Slides

# Original Sweeping Clock LLRF Implementation



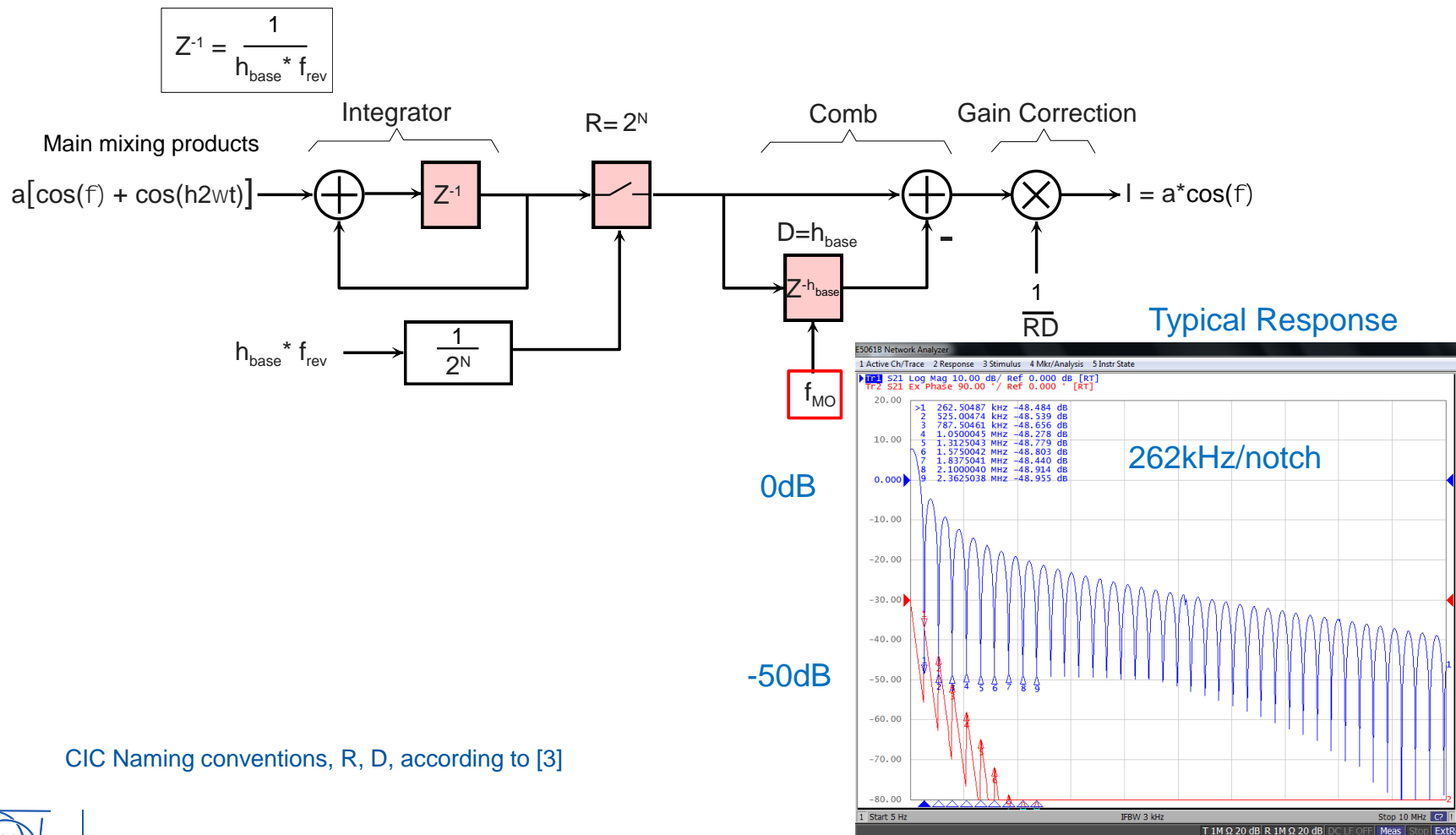
# Results

## Fixed Frequency operated CIC filter response (w.o. post-filter)



# Fixed Frequency Clock LLRF Implementation

## CIC Filter



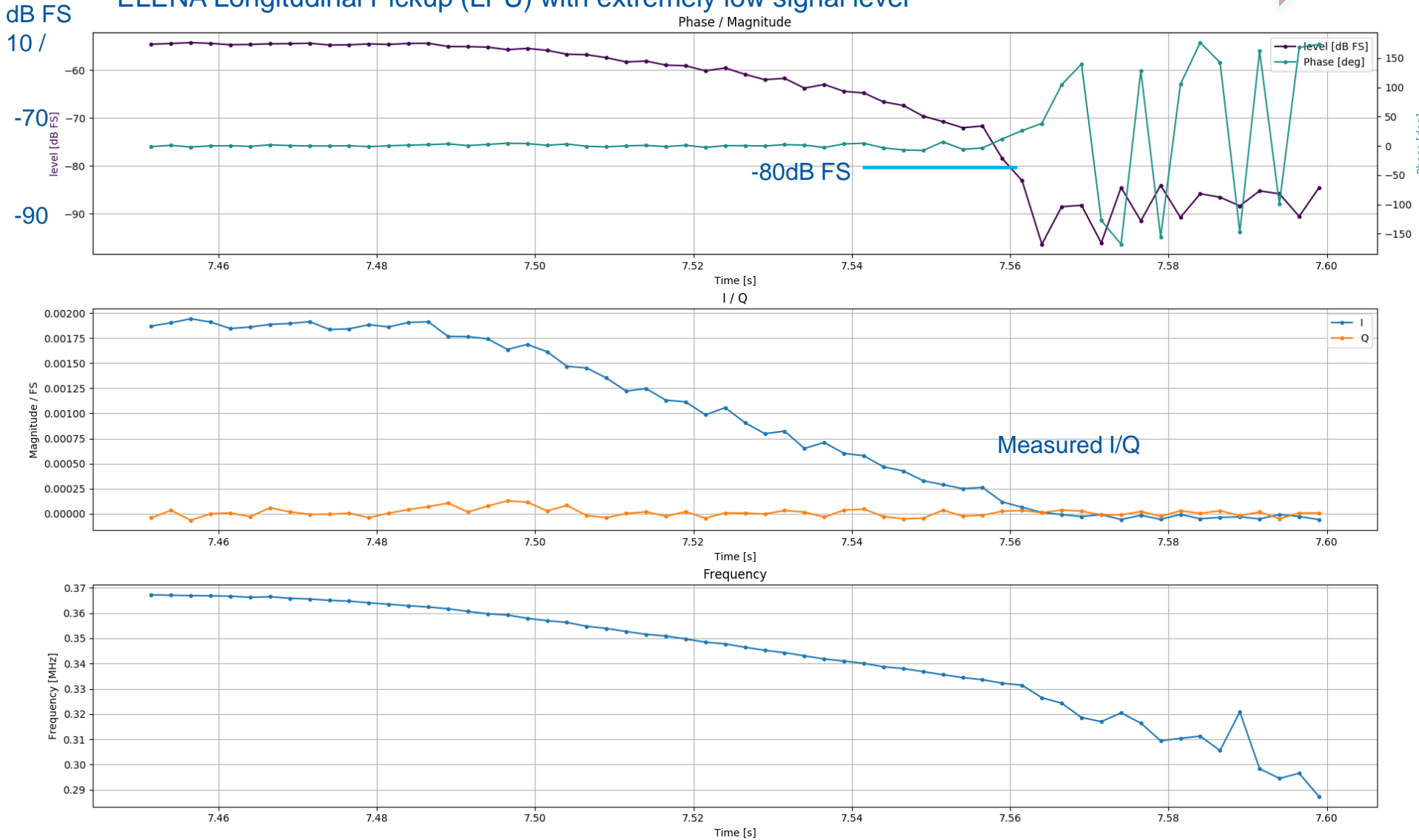
CIC Naming conventions, R, D, according to [3]



# Results

Beam Signal Lost 

## ELENA Longitudinal Pickup (LPU) with extremely low signal level





# Fixed Frequency Clock LLRF Implementation (4)

## CIC Bit Growth:

- Depends on the maximally expected decimation
- Depends of the differential delay

$$b_{grow} = \log_2(RD)$$

Bit growth for a first order CIC

Substituting R and D from slide 14 we get:

$$b_{grow} = N + \log_2\left(\frac{f_{FIX}}{f_{rev}}\right)$$

N = Differential delay shift control

Example:

- $b_{grow} = 14$
- $N = 0$

$$f_{rev} \geq f_{FIX} \frac{2^N}{2^{b_{grow}}} = \frac{122.7[MHz]}{2^{14}} = 7.5[kHz]$$

Example: smallest  $f_{rev}$  in ELENA decelerator  $\sim 140kHz$  ->  $N=4$  still allowed