
# LCLS-II LLRF Prototype Testing and Characterization

Larry Doolittle, Brian Chase, Joshua Einstein-Curtis, Carlos Serrano

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SLAC NATIONAL ACCELERATOR LABORATORY

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# Outline

- A little background on LCLS-II LLRF Design
  - DSP algorithms
  - Hardware partitioning
  - Frequencies
  - Thermal design
- Chassis performance
- Test results from FNAL CMTS
  - Field control
  - Resonance control
- Summary and parting comments

# Resonance Control and Quench Detect

Real and Imaginary component of $A$ (units $s^{-1}$) in cavity differential equation

$$\frac{d\vec{V}}{dt} = A\vec{V} + B\vec{K} + C\vec{I}$$

gives $Q_L$ and cavity detune frequency. Compute this inside FPGA for quench detect interlock and running the tuning loop.

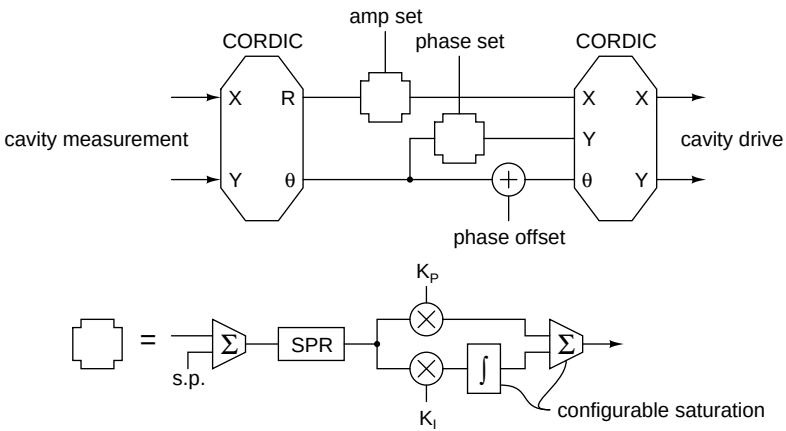
Explicitly (without beam)

$$A = \frac{1}{\vec{M}_V} \cdot \left[ \frac{d\vec{M}_V}{dt} - B'\vec{M}_K \right]$$

where $B'$ has to be calibrated *in situ*. Has been tested in hardware.

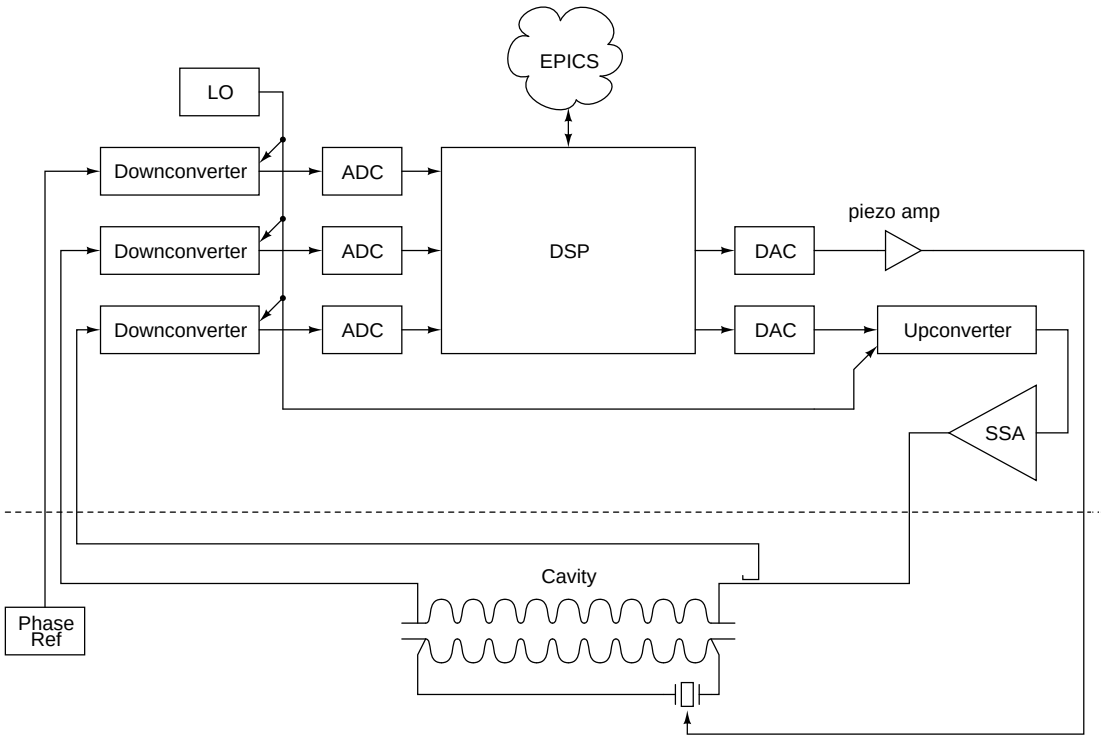
# Field control: SEL controller

- Real Delayen-style with amplitude and phase PI loops, smoothly turns itself into a GDR if there is enough forward power available
- Analog versions have a long history
- Similar digital version used at JLab
- Well-exercised in simulation

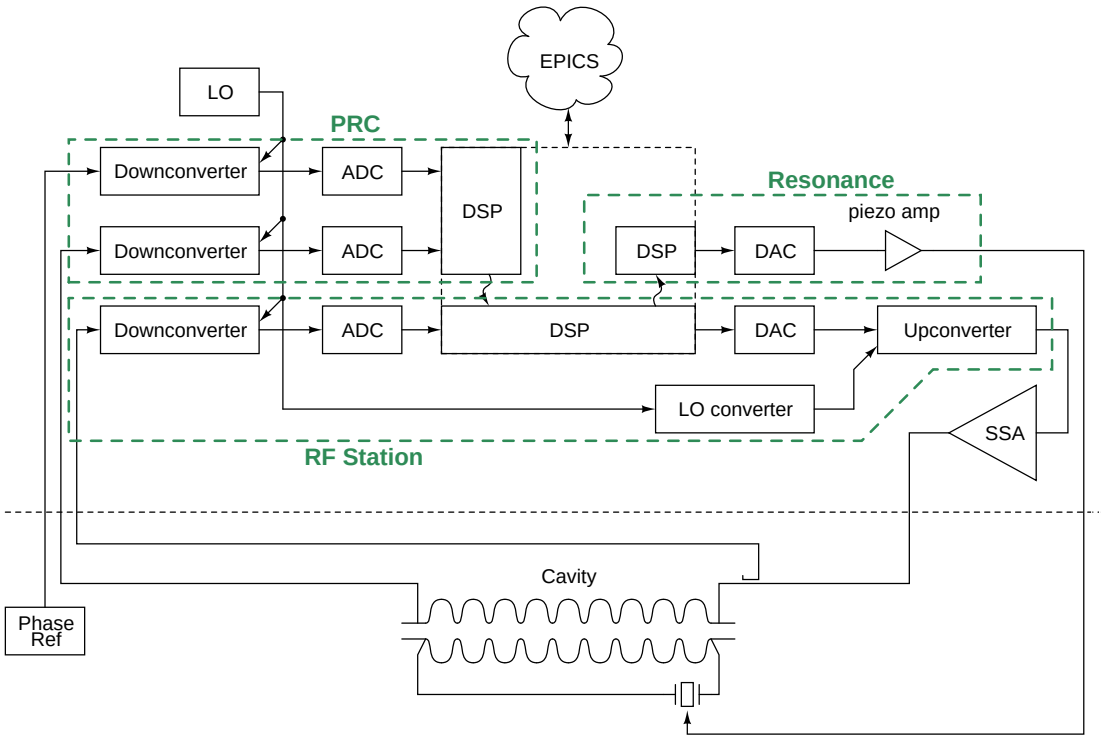



Simplified block diagram of DSP path for field control loop

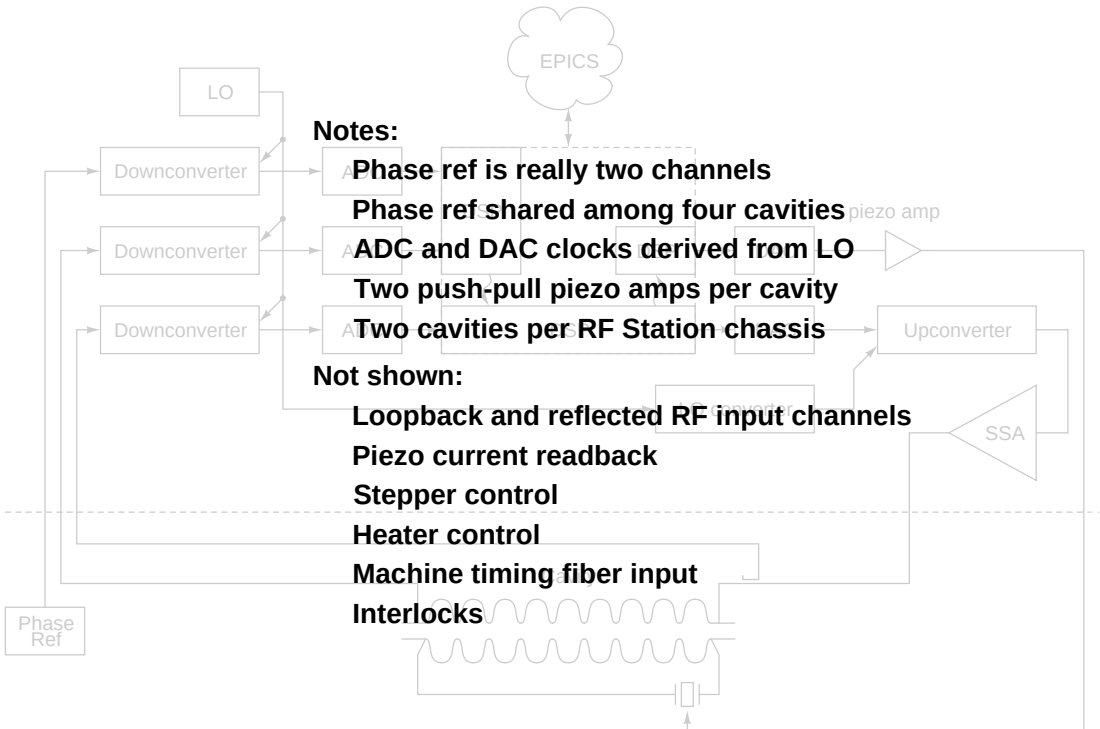
# Simplified hardware architecture



# Simplified hardware architecture



# Simplified hardware architecture




**Notes:**

- **Phase ref is really two channels**
- **Phase ref shared among four cavities**
- **ADC and DAC clocks derived from LO**
- **Two push-pull piezo amps per cavity**
- **Two cavities per RF Station chassis**

**Not shown:**

- **Loopback and reflected RF input channels**
- **Piezo current readback**
- **Stepper control**
- **Heater control**
- **Machine timing fiber input**
- **Interlocks**

# Frequency Relationships for Near-IQ Sampling

$$
\begin{aligned}
f_{\mathrm{RF}} &= 1300\ \mathrm{MHz} \\
f_{\mathrm{Clk}} &= 94.3\ \mathrm{MHz} = f_{\mathrm{LO1}}/14 \\
f_{\mathrm{IF1}} &= \ \ 20\ \mathrm{MHz} = f_{\mathrm{Clk}} \cdot \tfrac{7}{33} \\
f_{\mathrm{LO1}} &= 1320\ \mathrm{MHz} = f_{\mathrm{RF}} \cdot \tfrac{66}{65} \\
f_{\mathrm{IF2}} &= \ 145\ \mathrm{MHz} = f_{\mathrm{Clk}} \cdot \tfrac{203}{132} \\
f_{\mathrm{LO2}} &= 1155\ \mathrm{MHz} = f_{\mathrm{LO1}} \cdot (1 - \tfrac{1}{8})
\end{aligned}
$$

**Unusual Split-LO design bypasses usual compromises in choosing IF**

- Low 20 MHz IF for receiver reduces crosstalk & sensitivity to ADC clock jitter
- High 145 MHz IF for transmitter improves output sideband-select filter
- Circumvents usual problems with isolation between drive and input IF
- Receiver IF near middle of first Nyquist zone of 94.3 MS/s ADC
- Full $\mathrm{TM}_{010}$ passband (1274-1300 MHz) fits in first Nyquist zone of ADC
- Transmitter IF near middle of second Nyquist zone of 188.6 MS/s DAC

# Thermal Design

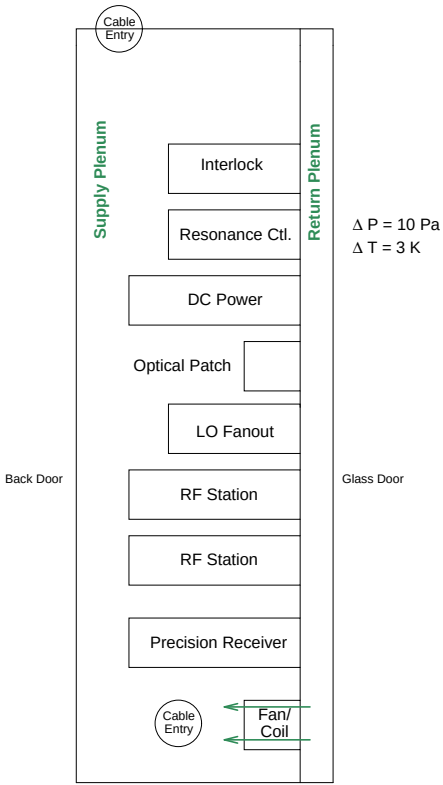
One rack supports 4 cavities

Total chassis power dissipation estimate/budget:
$\sim$50 W/chassis $\times$ 5

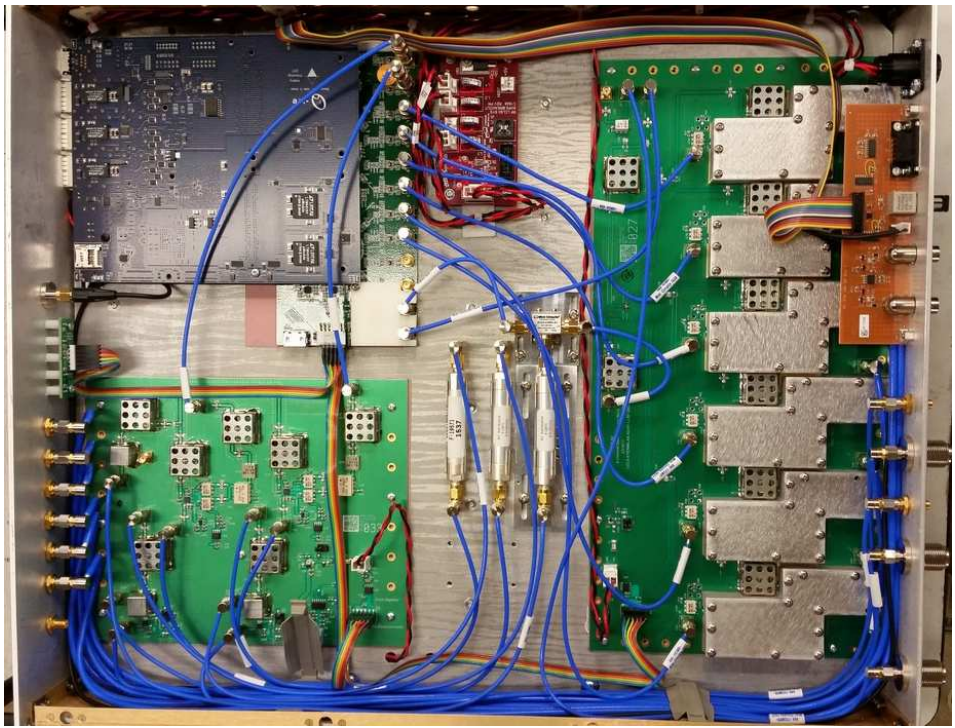
250 W / 3 K / $\rho c_P$ = 0.064 $m^3$/s

0.064 $m^3$/s $\cdot$ 10 Pa = 0.64 W

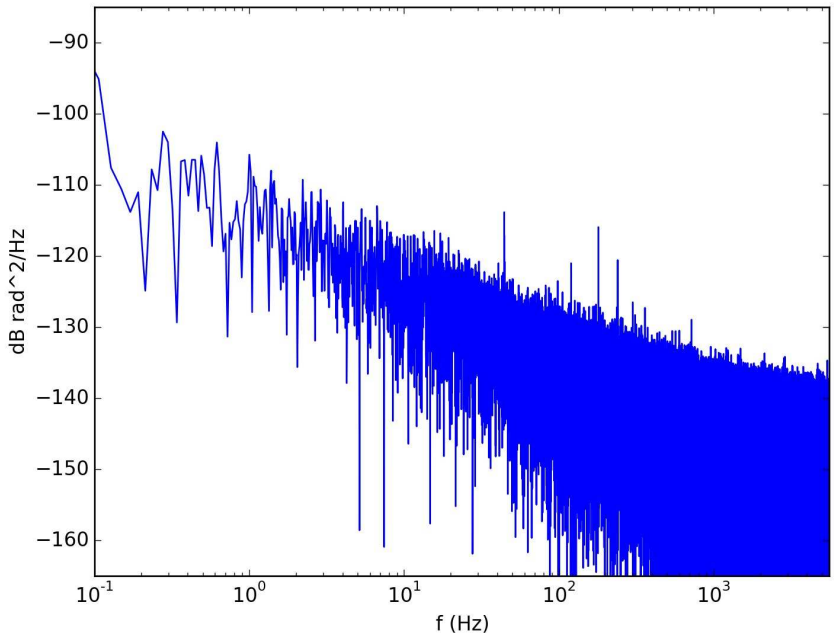
Front of rack can be opened for access to test points, without totally breaking airflow pattern and thermal management



# Chassis assembled

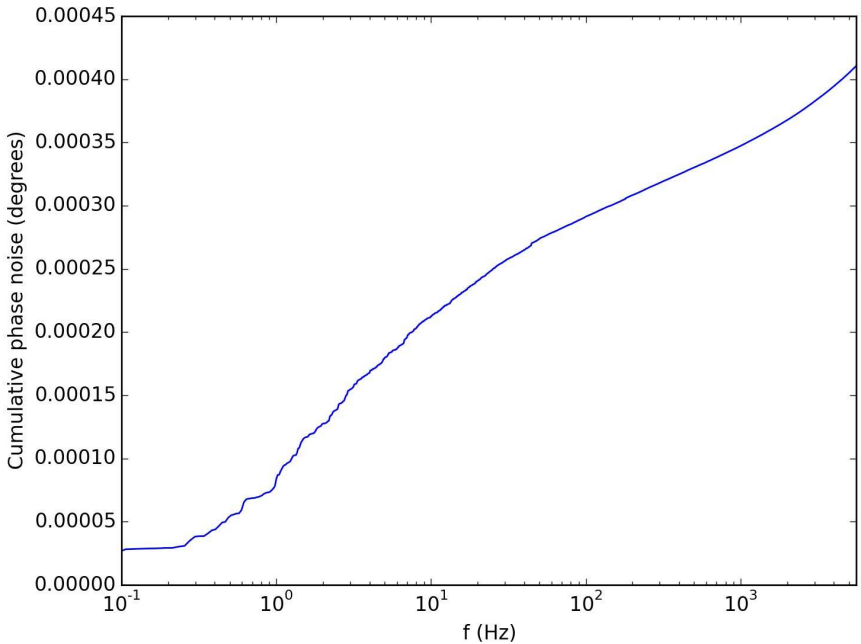


# Chassis phase noise




Measured at 1300 MHz using passive splitter and short cables to two Rx inputs.

# Chassis phase noise




Note 1 Hz high-pass included to represent beam-based feedback and to avoid logarithmic singularity of $1/f$ noise integral to DC.

# Rack-under-test installed at FNAL CMTS

Power supply

Resonance control

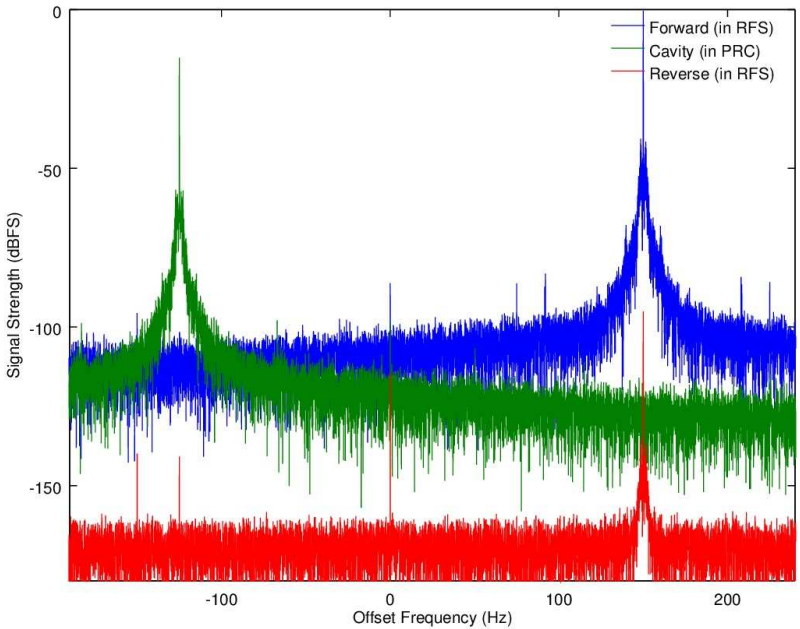
reserved

RF Station

RF Station

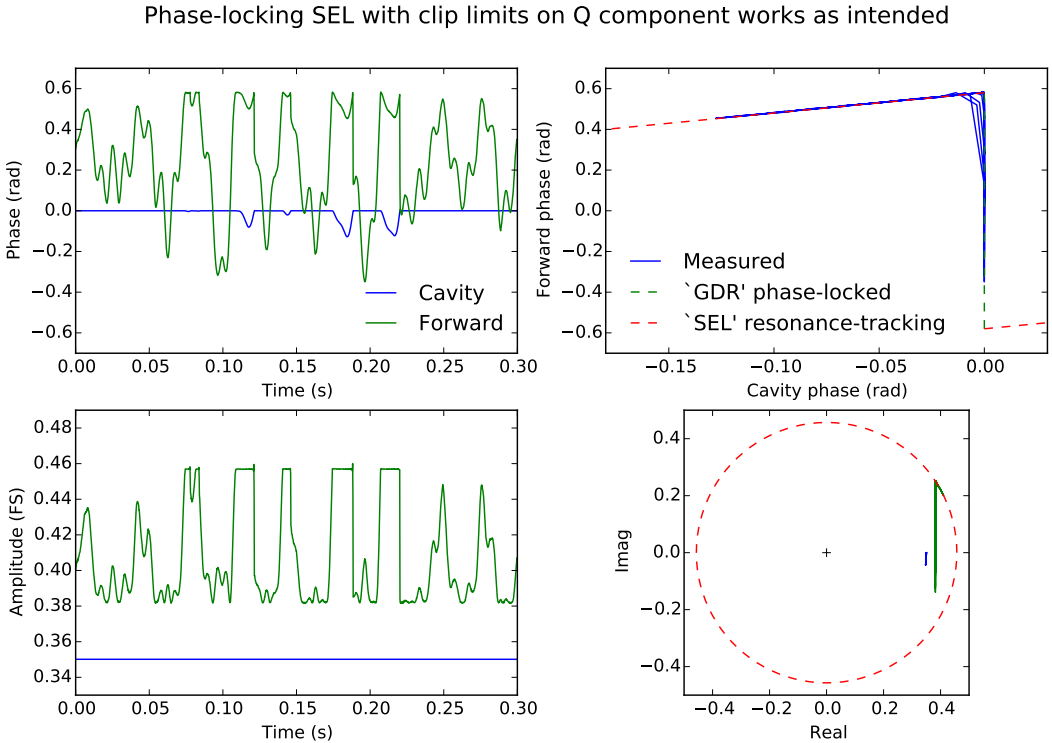
Precision Receiver

# Crosstalk

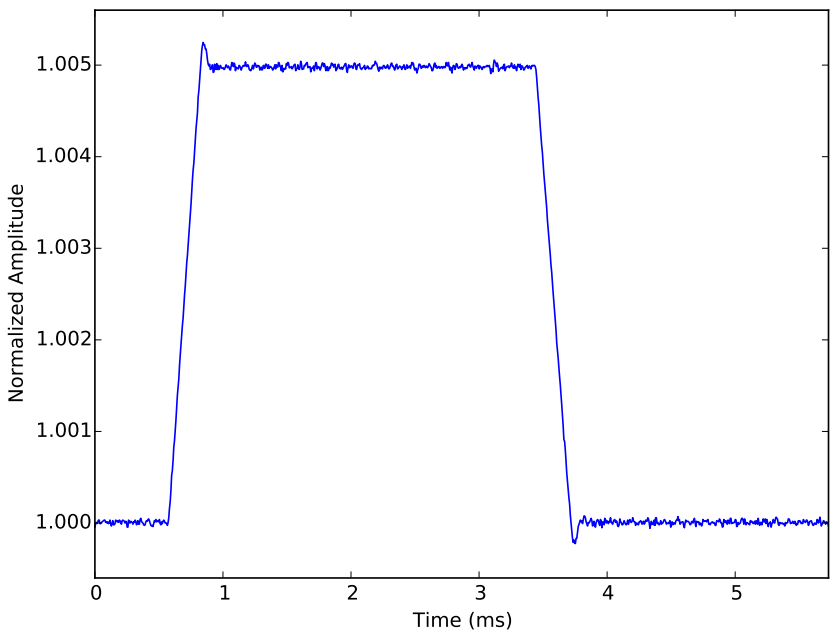



Intrachassis crosstalk -90 dB, interchassis crosstalk better than -120 dB

# Phase-locking SEL w/IQ-clip works as intended

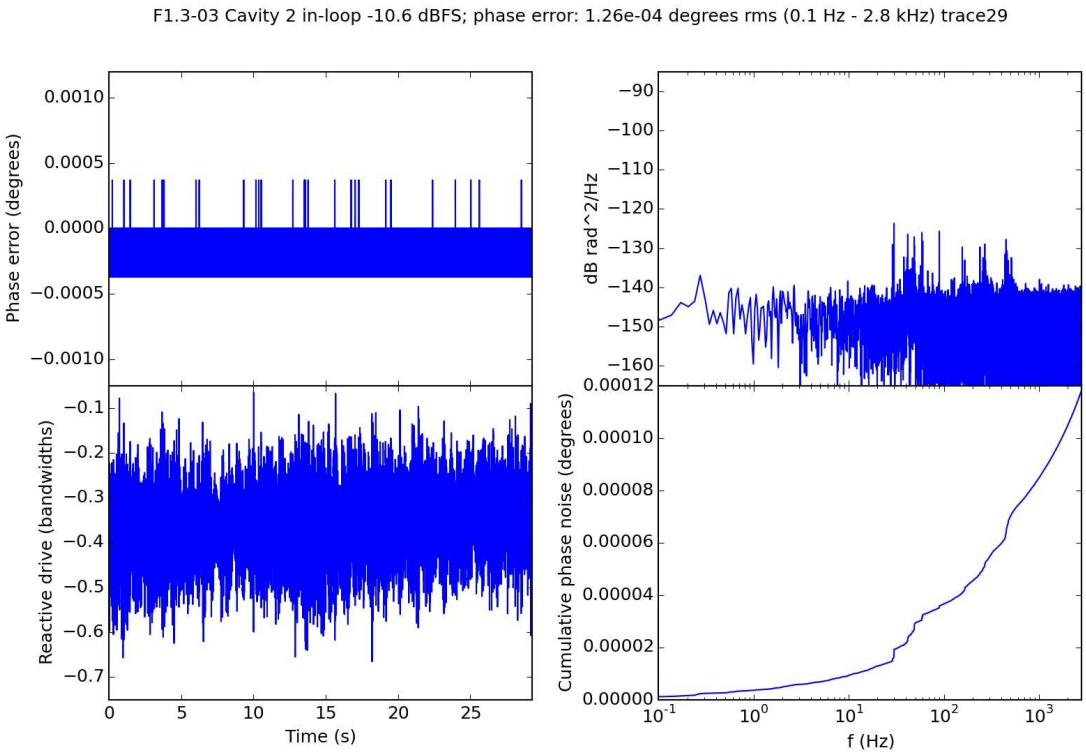


# PI Gains can be set for reasonable transient

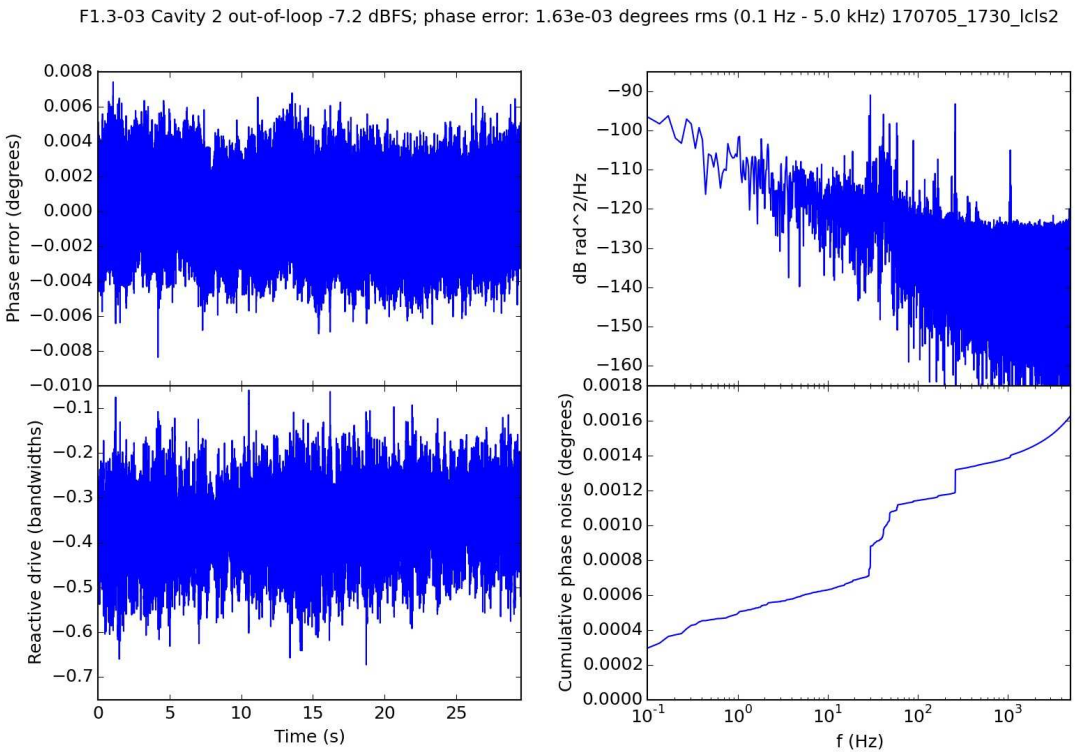



Response to 0.5% amplitude step in setpoint, slew-rate-limited due to clip limits and cavity pole.

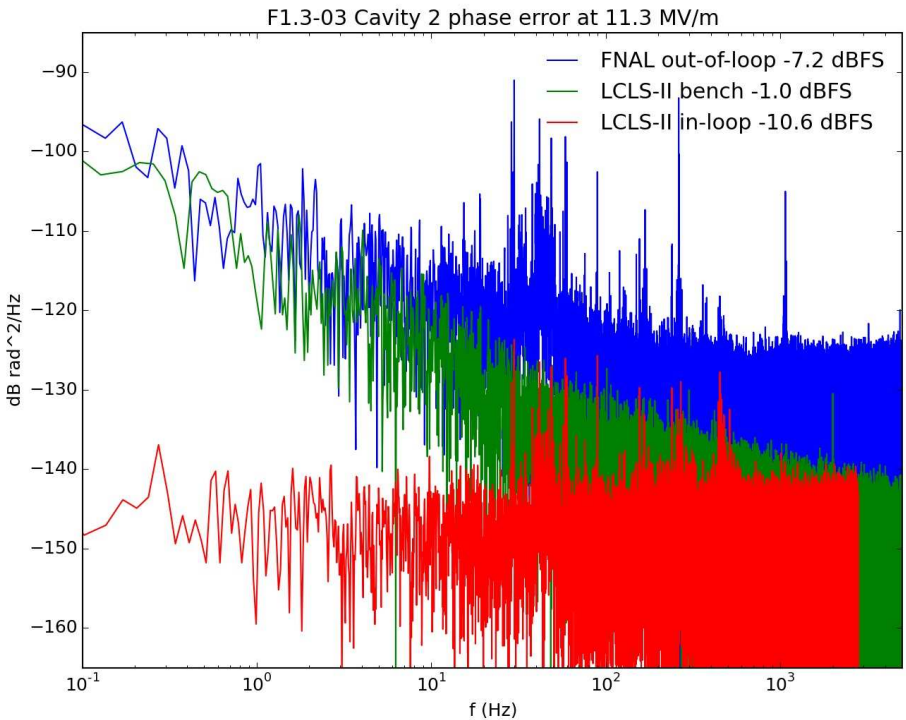
# In-loop phase noise



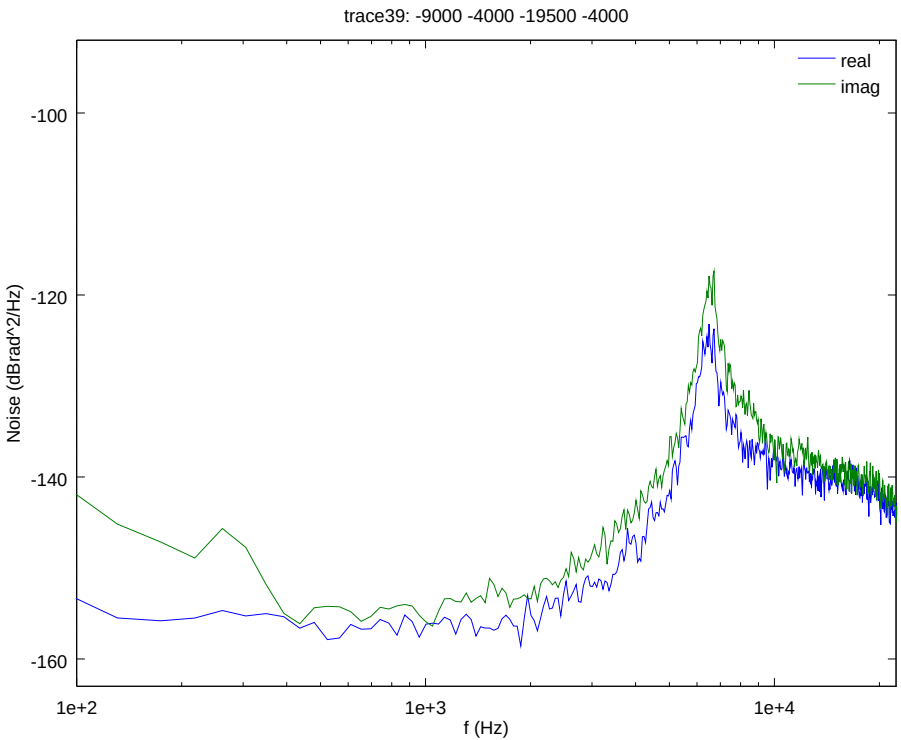
# Out-of-loop phase noise



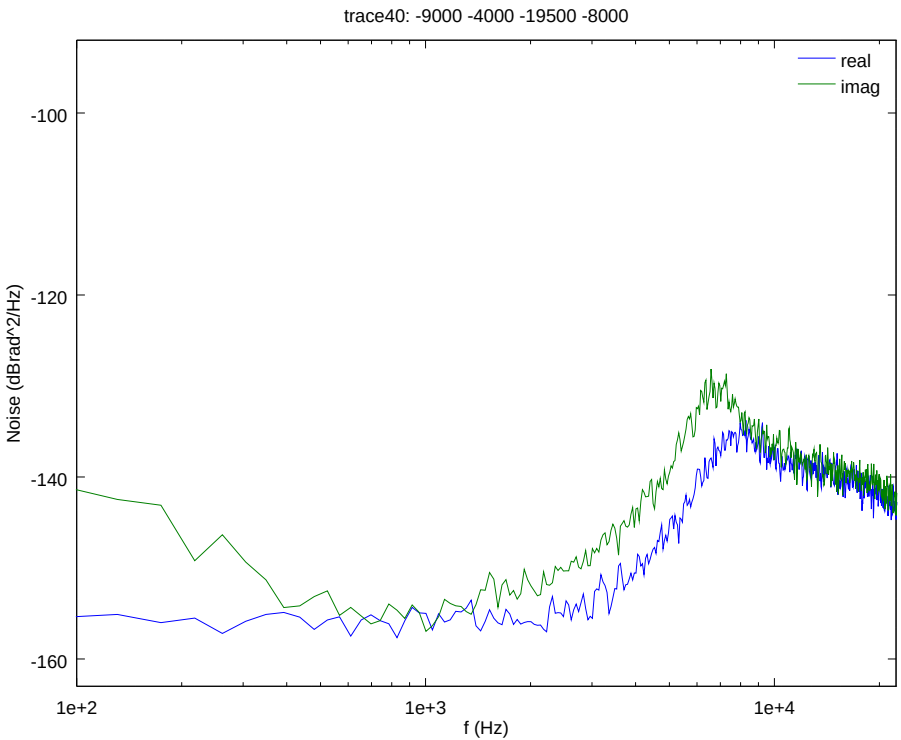
# Phase noise comparison



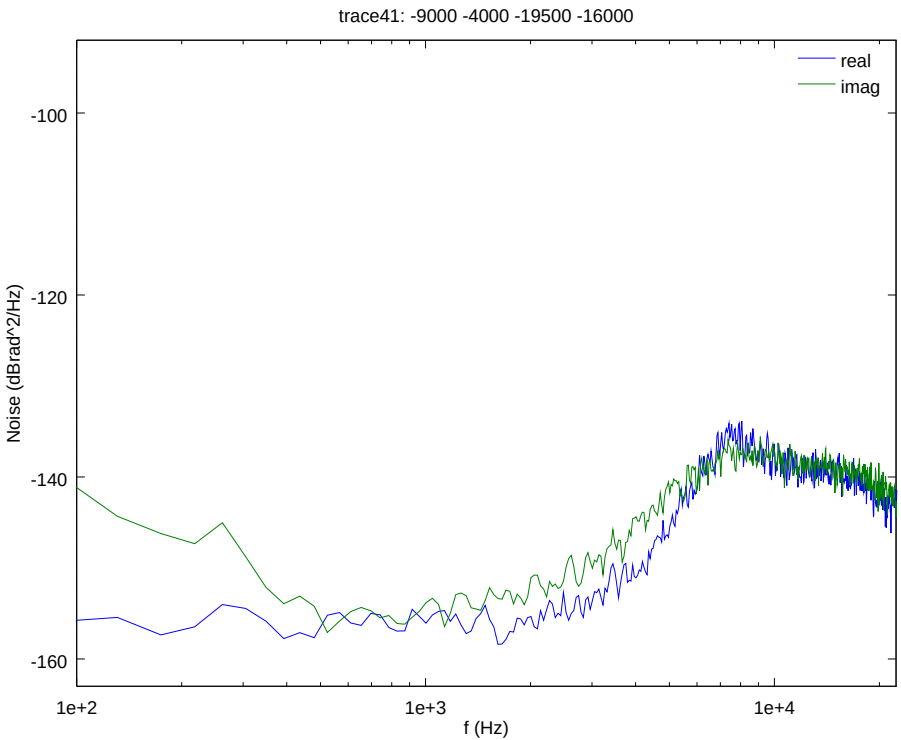
# Phase noise near closed-loop bandwidth, $K_P \approx 150$



# Phase noise near closed-loop bandwidth, $K_P \approx 300$



# Phase noise near closed-loop bandwidth, $K_P \approx 600$



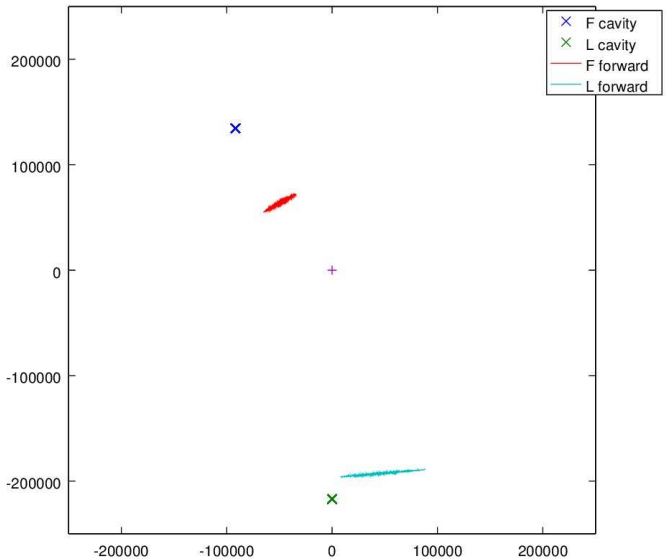
# Cavity Phase noise spectra comments and *caveats*

- Signal strengths are different for the three curves
- 11.3 MV/m was administrative limit for that testing session
- Crosstalk from forward and reverse probes in FNAL system explains amplitude discrepancy for microphonics peaks; corresponding crosstalk on LCLS-II system is demonstrated $<$ -129 dB
- $1/f$ components appear as expected
- FNAL CMTS installation not set up to test drift behavior

**Superficial conclusion is not wrong:**

- Field out-of-loop error $<$ 0.018° peak-peak, 0.0016° rms, in 0.1 Hz to 5 kHz, better than spec; leaves margin for:
  - larger closed-loop bandwidth (goal 20 kHz)
  - phase-reference-line contribution
  - beam-loading effects
  - larger microphonics (this cavity had about 60% of detuning "spec")
  - unknowns

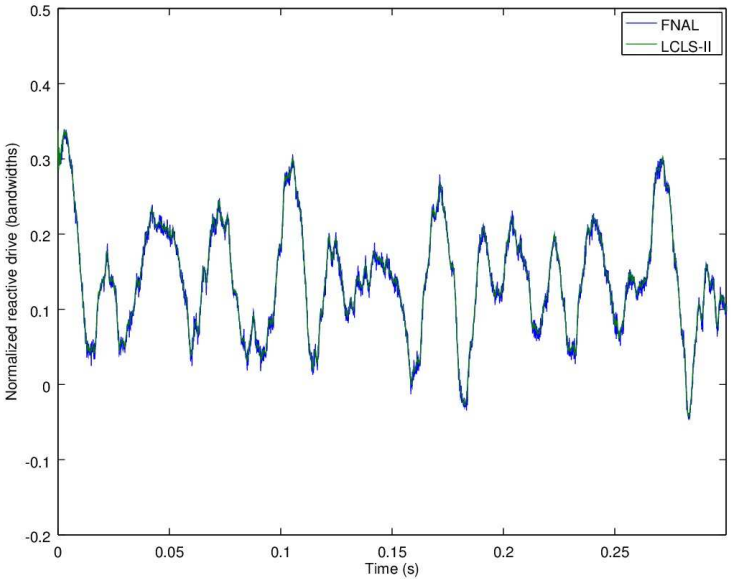
# Detune input data




Two independent systems (sharing LO) collecting cavity and forward

Unknown relative phases and calibration

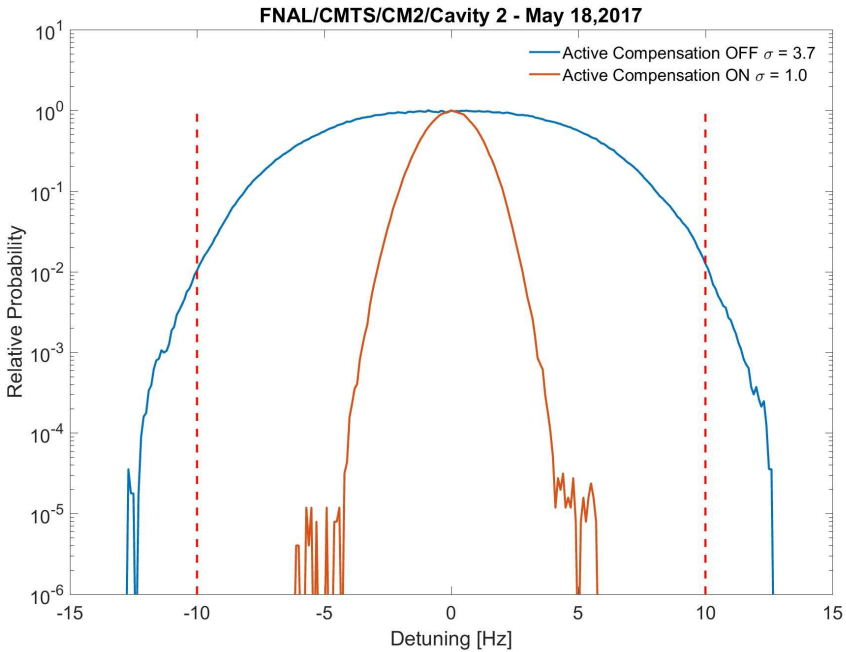
# Detune normalized result




Two independent systems (sharing LO) collecting cavity and forward

One hand-fit parameter, to time-align the two data sets

# Active Resonance Control experiments




Resort to this **after** running out of passive vibration control measures

# Resonance Control

Many pieces tested individually:

- RFS measures detune frequency, independent of phase-locking
- Fiber communcation from RFS to Resonance chassis
- DSP filter banks set up to suppress microphonics peaks (and DC mistuning)
- Piezo interface FPGA programming and hardware driver

Now it's a simple matter of running all those things simultaneously, and testing.

# Conclusion

Tests on Prototypes give evidence this system meets stringent performance specs based on the high quality electron beam needed for an X-ray light source

More testing is (always) needed, still software to debug

Architecture is modern and modular, will form a reliable and operable part of the larger LCLS-II controls.

**Thank You!**
**Gracias!**


**LCLS-II LLRF Collaboration Team**

K. Campbell, L. Doolittle, Q. Du, G. Huang, J. Jones,
C. Serrano, V. Vytla, **LBNL**
S. Babel, A. Benwell, M. Boyes, G. Brown, D. Cha, G. Dalit, J. DeLong,
J. Diaz-Cruz, B. Hong, R. Kelly, A. McCollough, A. Ratti, C. Rivetta, **SLAC**
R. Bachimanchi, C. Hovater, D. Seidman, **JLab**
B. Chase, E. Cullerton, J. Einstein, D. Klepec, **FNAL**

# Field Control

Nominal setup that's expected to produce 0.01° / 0.01% total performance:

- 10 Hz detuning represents 0.62 reactive component, .62/.004° → 79 dB goal
- 20 kHz zero-dB crossing, with 16 Hz cavity bandwidth, 62 dB $P$ gain
- 5 kHz control-system zero (transition to $I$ gain), can give 34 dB additional gain at a hypothetical 100 Hz microphonic line (96 dB total, large but not crazy)
- 300 $\mu$A step = 12 MV → 0.75 unitless transient
- Unit current loading step produces 0.07% error, 300 $\mu$A step → 0.05%

  → need feedforward to cut effect by factor of 12

  expect the beam stays in the pipe without feedforward

That's ideal-world physics and textbook control theory

- choose to build hardware with some margin, can at least scan gains and stay textbook-stable up to 40 kHz zero-dB crossing

Broadband feedback means fast recovery from transient events (gnome-kicks)

# ADC selection

- $>$ 94.3 MS/s (hard limit)
- $<$ -155 dBc NPD (goal)
- $>$ 95 dB crosstalk at 20 MHz (goal)
- $<$ 200 ns latency (goal)
- differential signalling
- density and FPGA pin usage suited for sane construction and interfacing of 8-in 2-out board "value engineering"

| | density | interface | SNR | P/ch | crosstalk[1] | latency[2] |
|---|---|---|---|---|---|---|
| LTC2175 | 4× | LVDS-ser | 73.1 dB | 140 mW | -84 dB | 6 |
| AD9253 | 4× | LVDS-ser | 75.2 dB | 110 mW | -106 dB | 16 |
| **AD9653** | **4×** | **LVDS-ser** | **77.8 dB** | **164 mW** | **-102 dB** | **16** |
| AD9268 | 2× | LVDS-par | 78.2 dB | 375 mW | -109 dB | 12 |
| LTC2107 | 1× | LVDS-par | 79.7 dB | 1280 mW | N/A | 7 |
| AD9656 | 4× | JESD204B | 79.9 dB | 197 mW | -104 dB | 29+ |
| AD9650 | 2× | LVDS-par | 80.0 dB | 390 mW | -109 dB | 12 |

1. Estimated at 20 MHz
2. Cycles

# Rejected exotic ADC techniques

- Multiple receiver/ADC lanes per cavity
  - 2× allows separation of Rx noise spectrum *vs.* cavity noise spectrum
  - 3× gives per-channel measurement of Rx noise spectrum
  - also 3 dB or 5 dB increased SNR
  - also 3 dB or 5 dB more in-chassis LO power
- Higher-end ADCs have as much as 4 dB better NPD, but need
  - many more FPGA pins, or high-speed-serial pins
  - more painful board layout and fab
  - more expensive FPGA
  - more heat dissipated near analog components

# Feedback performance depends on group delay

| Group delay (ns) | ≡ latency |
|---|---|
| 50 | input analog BPF |
| 170 | ADC pipe (16 cycles at 94.3 MHz) |
| 64 | Precision Rx DSP (12 cycles at 188.6 MHz) |
| 140 | GTP and fiber latency |
| 106 | Controller DSP (20 cycles at 188.6 MHz) |
| 1000 | bandpass filter in DSP (160 kHz) |
| 70 | notch filter in DSP ($\sim$800 kHz for $8\pi/9$ mode) |
| 40 | DAC (7 cycles at 188.6 MS/s) |
| 20 | sideband selection filter |
| 170 | Estimated SSA |
| 100 | cables and waveguides |
| 70 | contingency |
| 2000 | total, can sustain 40 kHz closed loop bandwidth |