Low Level RF for PIP-II

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PIP-II LLRF Team

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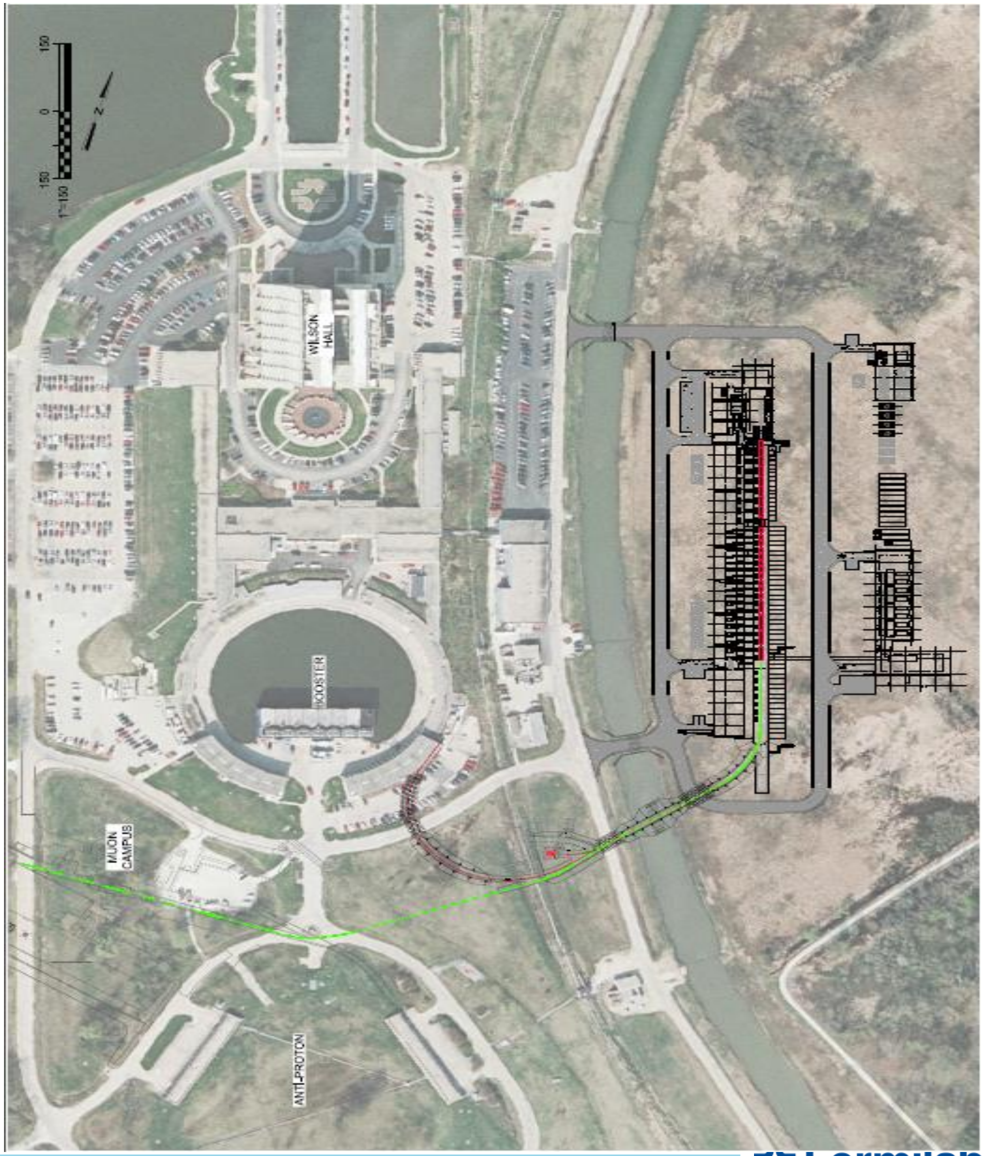
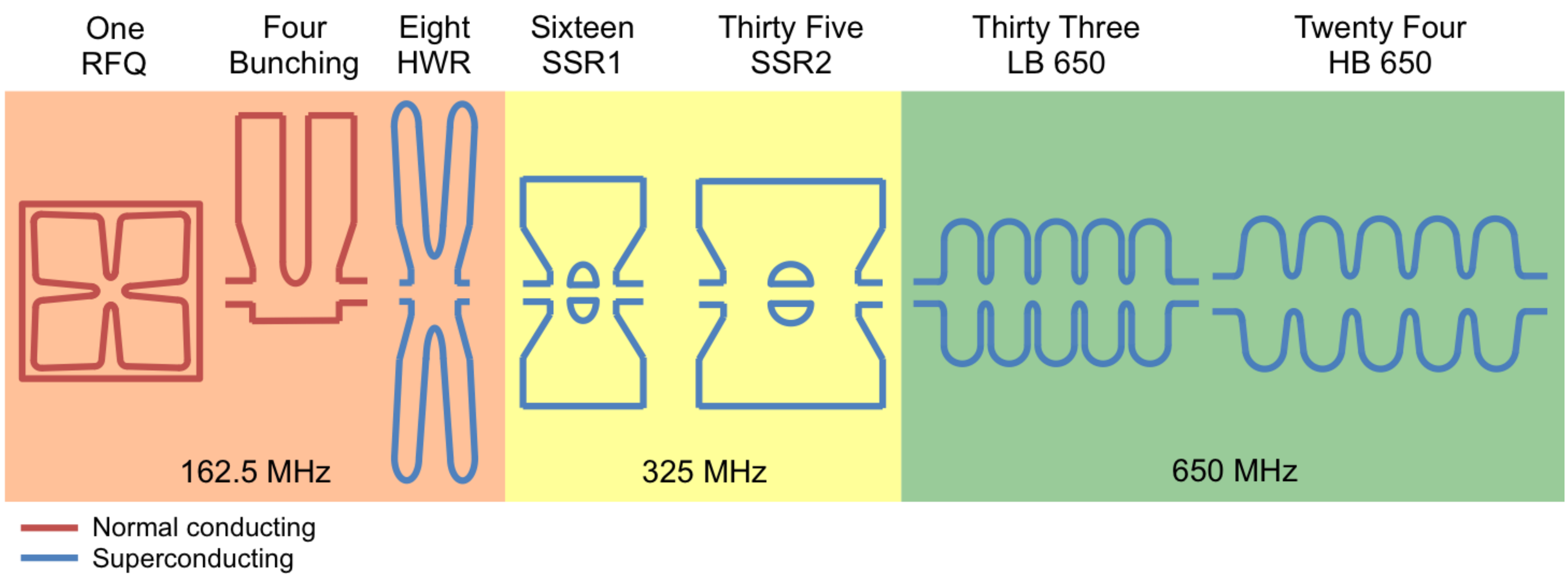
What is PIP-II

- PIP – II is a 20Hz, 800 MeV, superconducting H- LINAC that will replace the existing 400 MeV copper LINAC
- The primary goal of this upgrade is to increase the beam power available to neutrino experiments to 1.2 MW
- As part of the PIP-II R&D plan we are also building a test stand
  - Warm front end, HWR, and SSR1
  - Goal to test the chopper and the transition from NC to SC as well as prove out accelerator technology



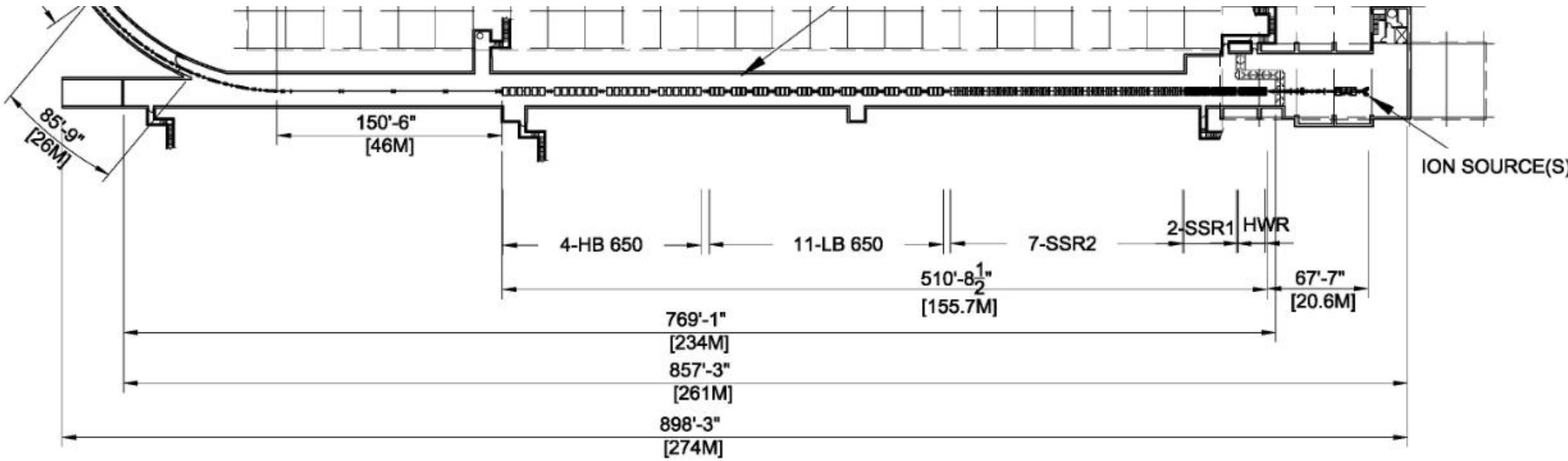
Overview of the PIP-II LINAC

- RF field control of all LINAC Cavities capable of pulsed and CW operation
- Multi-frequency Master Oscillator and Phase Reference lines
- Beam Chopper Waveform Generator
  - RF locking source for Booster during beam fill
  - Timing source
- Resonance control (microphonics and LFD)



Overview of the PIP-II LINAC

	Frequency [MHz]	Number of RF cavities	Amplifiers per Cavity	Pulsed / CW	Solid State Amplifier Power [kW]	Number of 4-cavity stations
RFQ	162.5	1	2	CW	75	1 (special)
Bunching Cavities	162.5	4	1	CW	3	1
HWRs	162.5	8	1	CW	3,7	2
SSR1s	325	16	1	Pulsed	7	4
SSR2s	325	35	1	Pulsed	20	9
LB650s	650	33	1	Pulsed	40	9
HB650s	650	24	1	Pulsed	70	6



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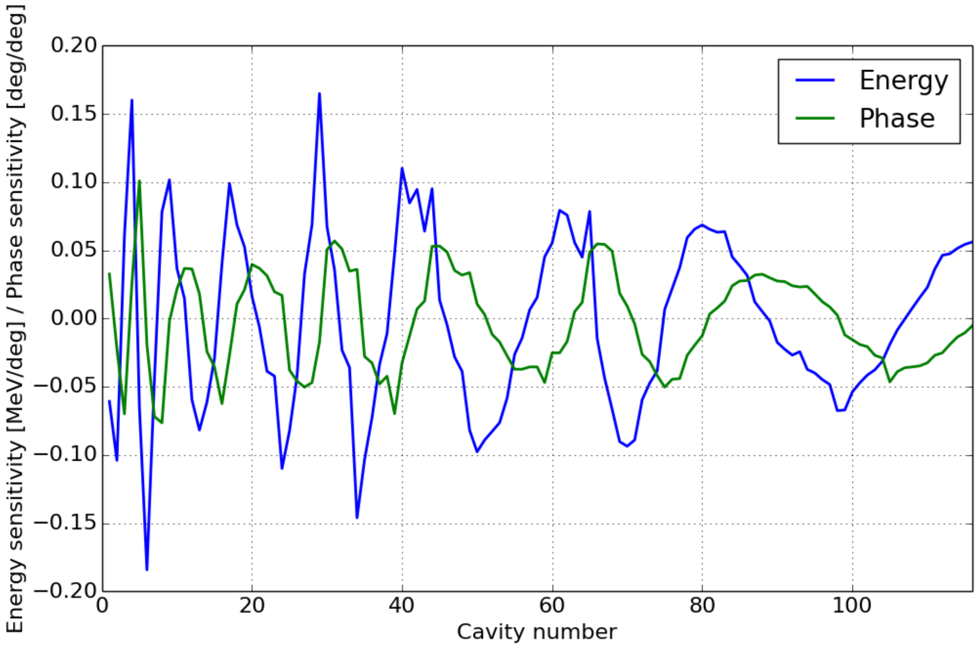

Energy and phase sensitivity at the end of the LINAC caused by perturbations to the phase of individual cavities.

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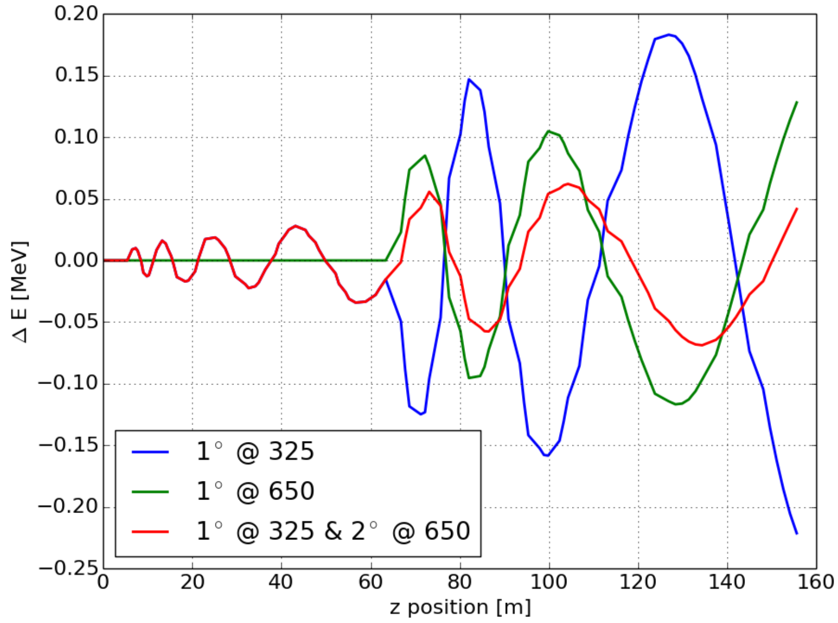

Energy sensitivity along the LINAC for phase errors introduced at frequency transitions: Here the phase errors are applied uniformly for each frequency type

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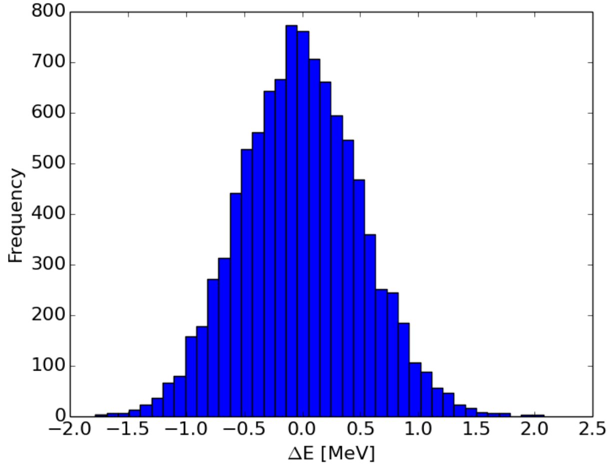

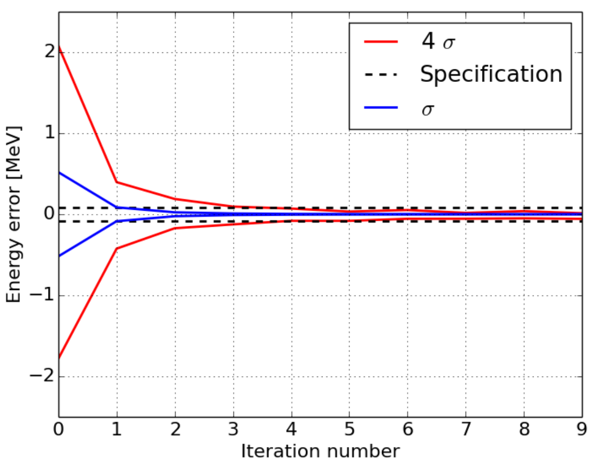

Assuming we can calibrate phase and amplitude to ±0.5° and ±1% respectively, we can stabilize the energy to 10^{-4} through pulse-to-pulse beam-based feedback using the last cryomodule.

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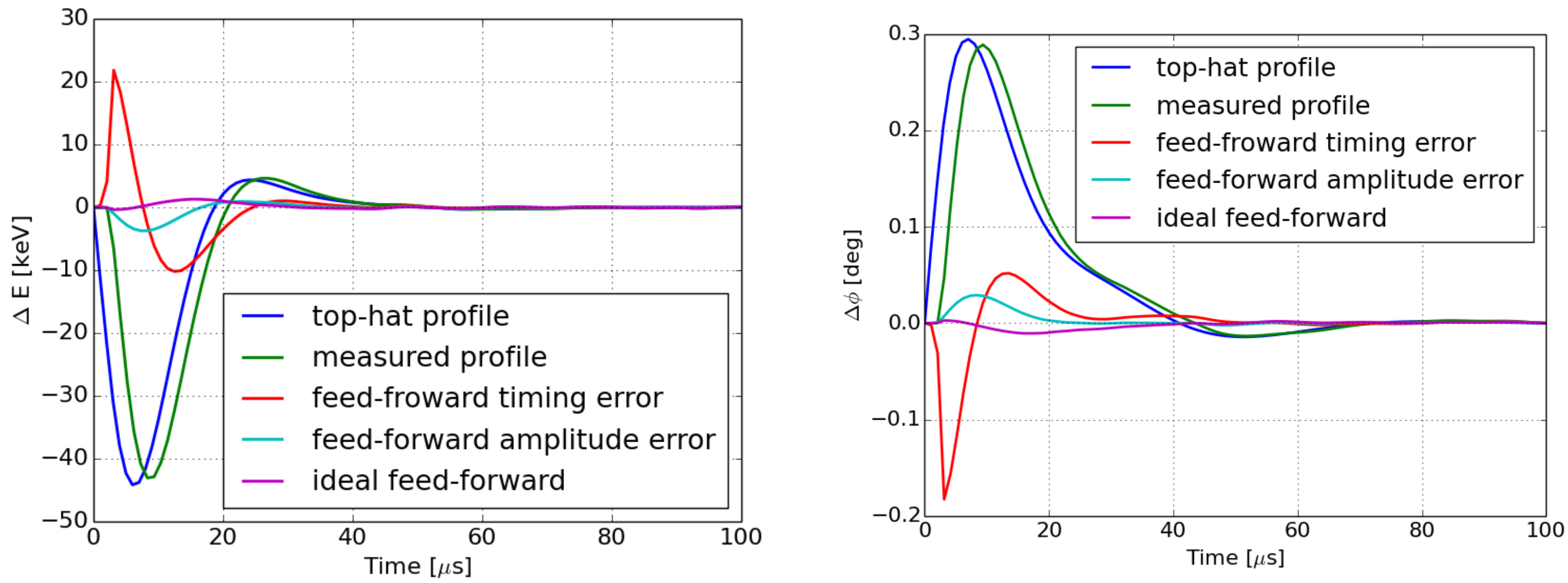


Resonance Control

- Resonance control specifications for each cavity type

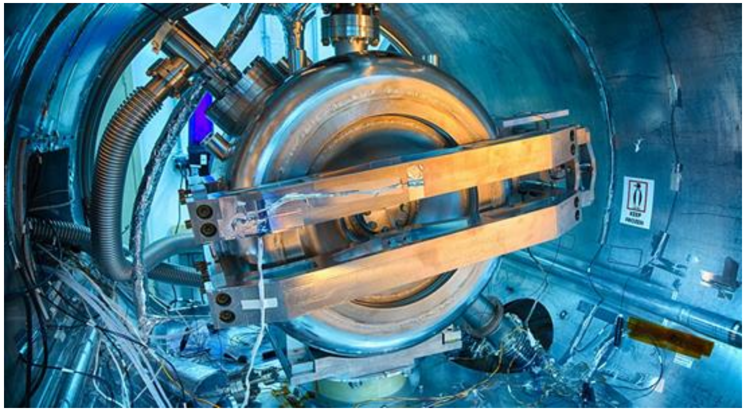
	HWR	SSR1	SSR2	LB650	HB650
Sensitivity to He pressure (FRS), *df/dP* , Hz/Torr	<25	<25	<25	<25	<25
… (measurements), *df/dP* , Hz/Torr	13	4.0	-	-	-
Estimated LFD sensitivity, df/dE^2, Hz/(MV/m)^2	-	-5.0	-	-0.8	-0.5
… (measurements), df/dE^2, Hz/(MV/m)^2	-1.5*	-4.4	-	-	-
Estimated LFD at nominal voltage (FRS), Hz	-	-500	-	-192	-136
… (measurements) at nominal voltage, Hz	-122.4	-440	-	-	-

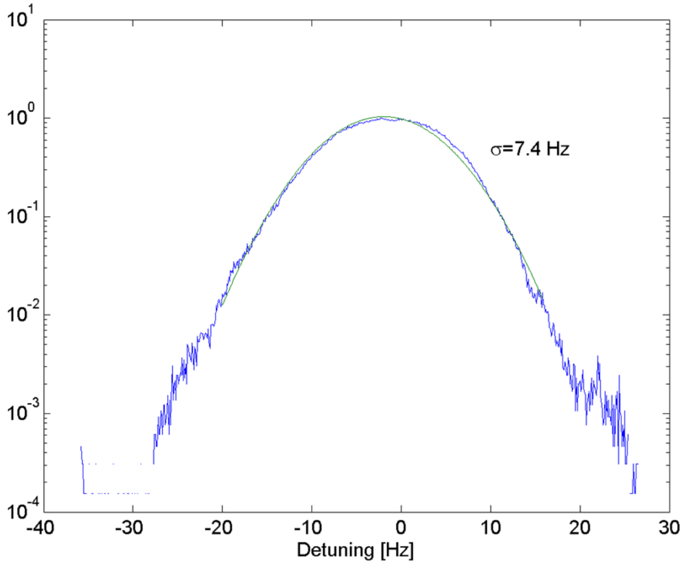
* Two cavities were measured in a test stand. The results are: -1.82 and -1.3 Hz/(MV/m)^2.

- Meeting these specifications will be challenging
  - Passive measures to reduce df/dp looks promising
  - Active compensation currently being tested on SSR1 type cavities

Active Resonance Control Testing

- PIP-II nominal operating conditions
  - 12.5 MV/m
  - 20 Hz repetition rate
  - 15% duty cycle, 0.5ms flattop
- STC operating condition
  - Greater than 12.5 MV/m
  - 25 Hz repetition rate
  - 7.5 ms fill, 7.5 ms flattop
- 7.4 Hz RMS detuning on the flattop
  - Specification is a peak detuning of 20 Hz: Further improvement is needed

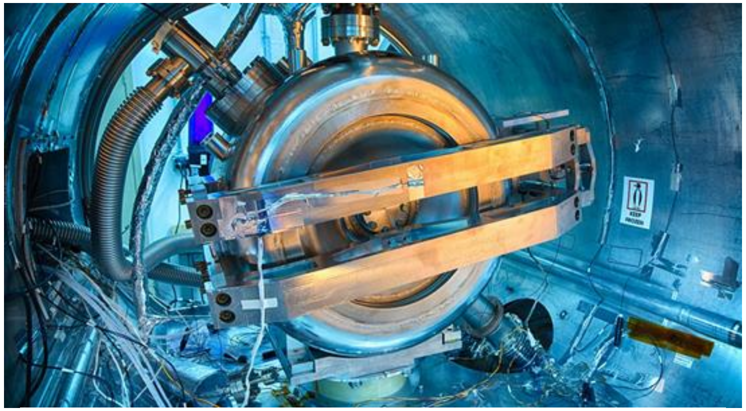


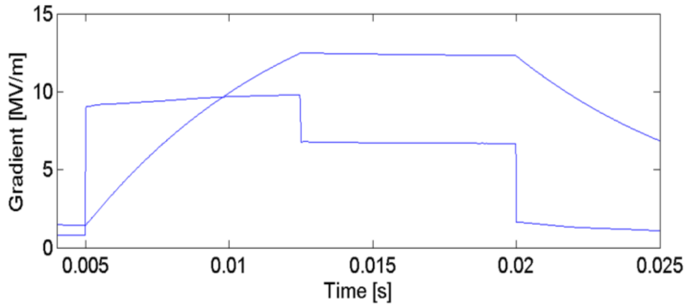


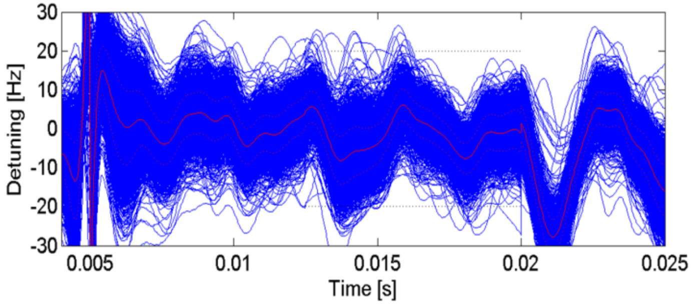
Active Resonance Control Testing

- Significant progress has been made toward PIP-II specification of detuning.

- Plan for incoming test at STC:
  - Improvements in feed back (automation of filter bank coefficients) should improve performance
  - May be possible to automatically extract optimal coefficients from delay scan data
  - Further firmware improvements should allow more detailed studies of pulse structure



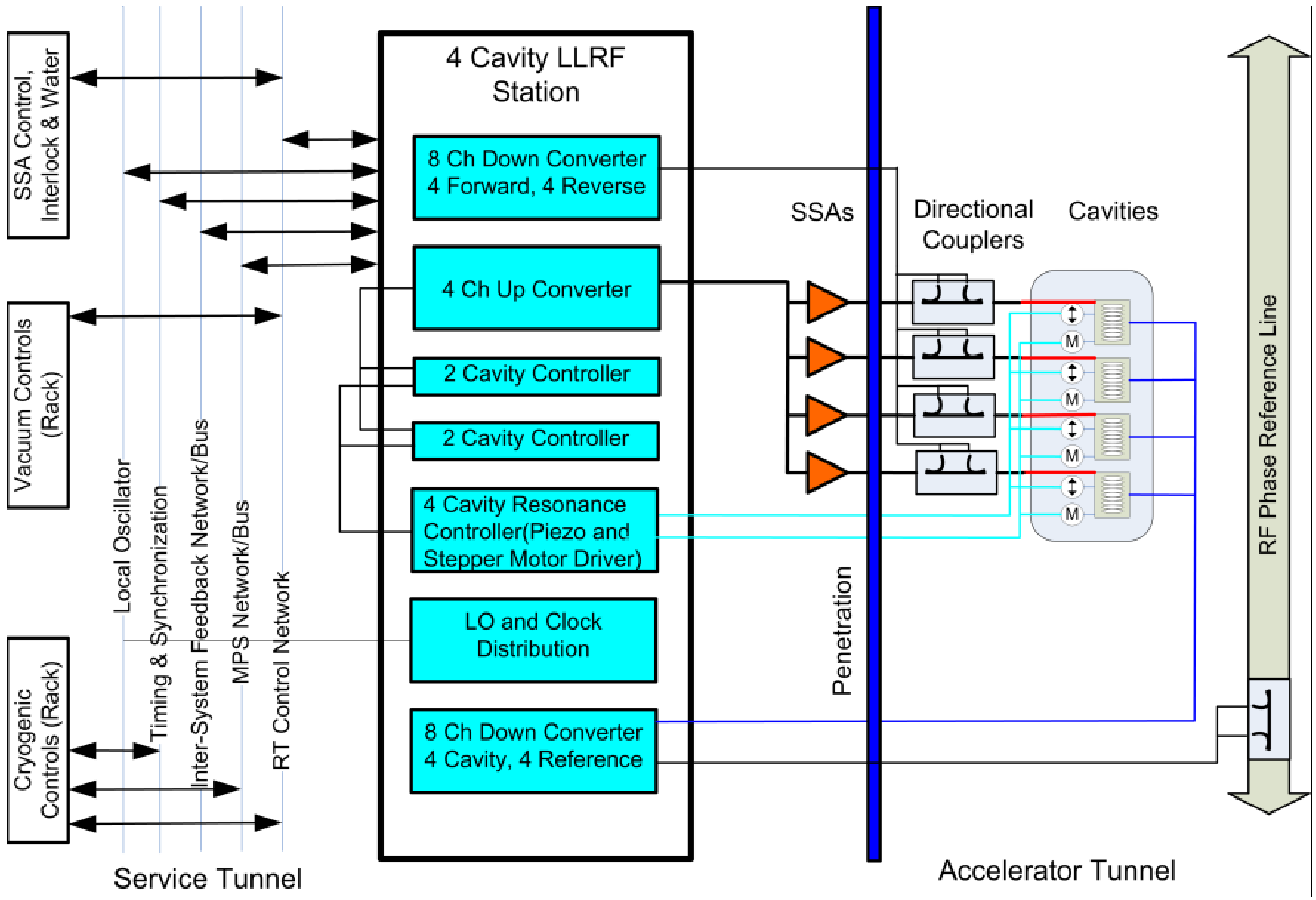




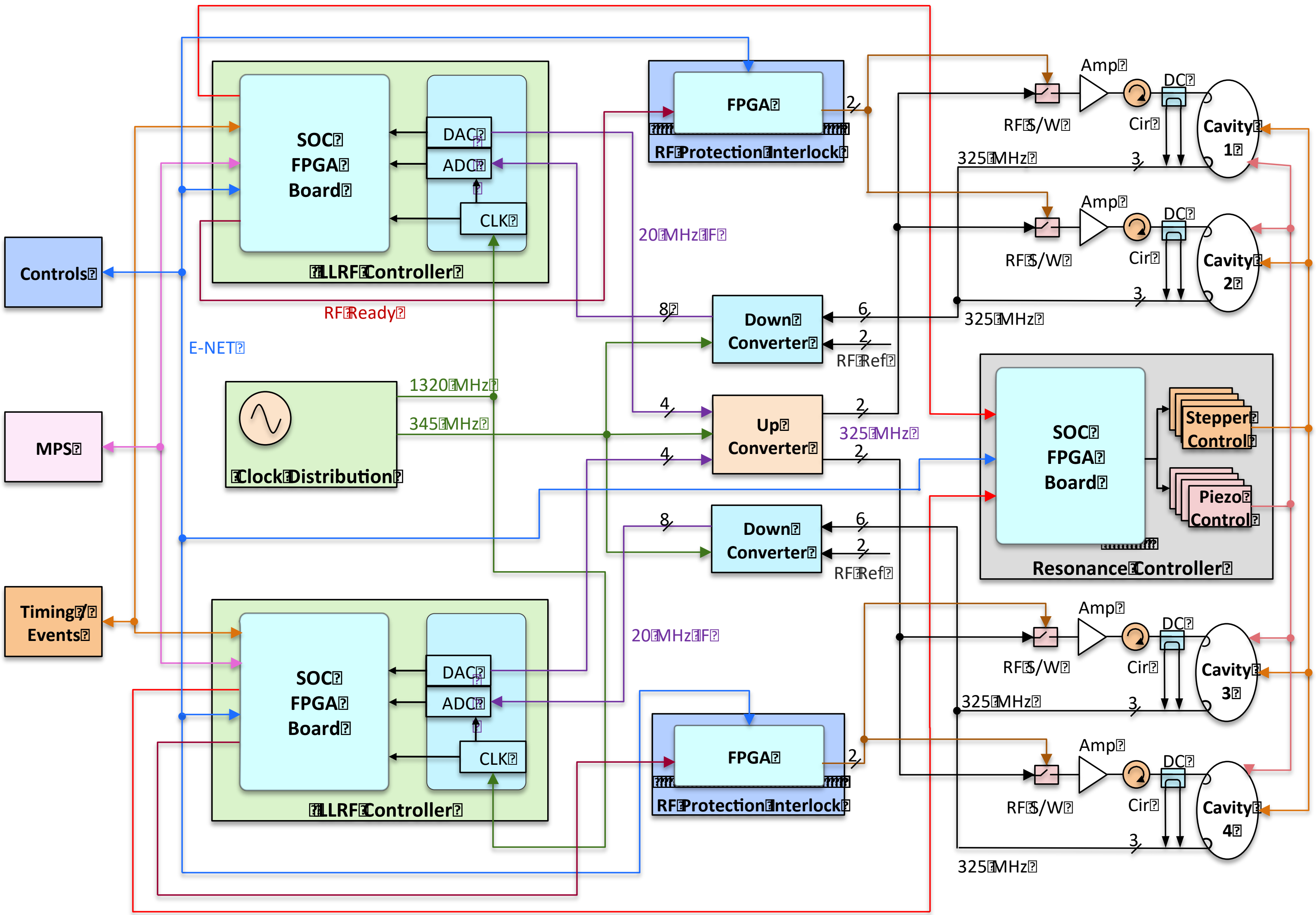
System conceptual design

Rack layout and module descriptions

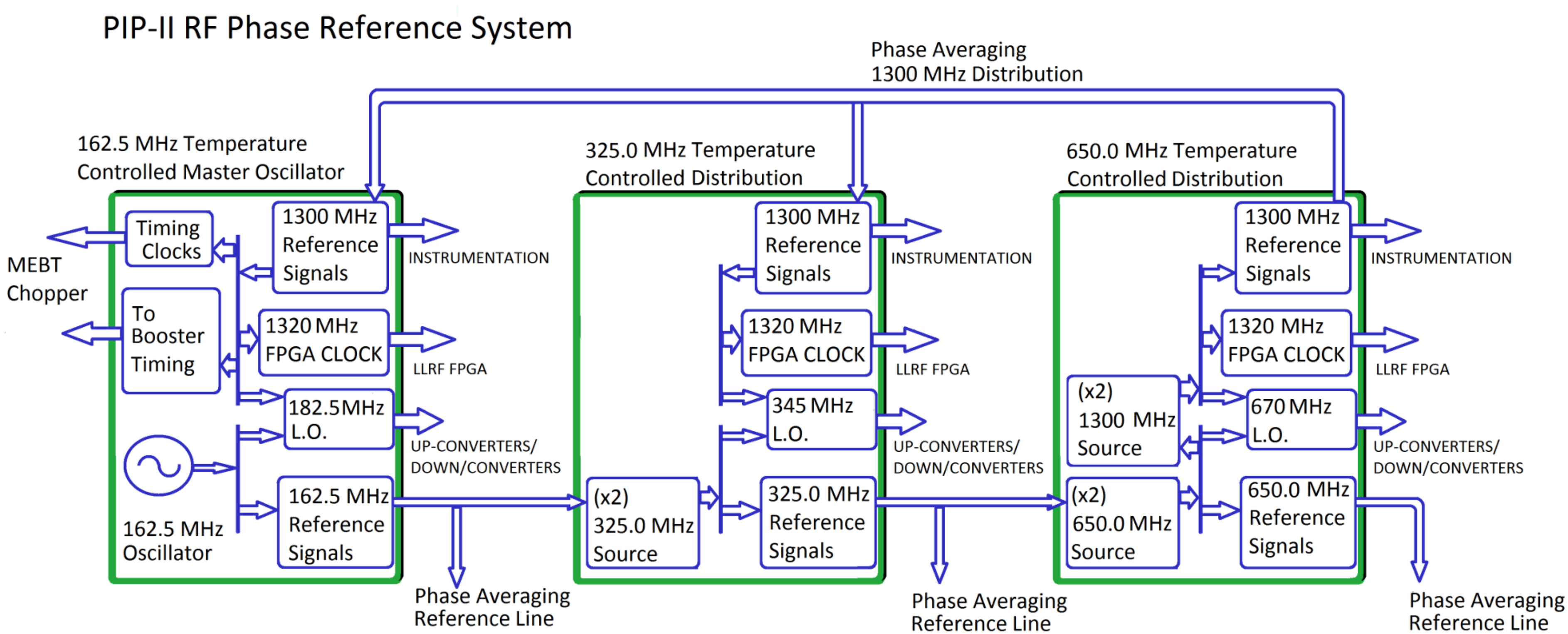
LLRF System for PIP-II



LLRF Signal Chain for 4 cavities

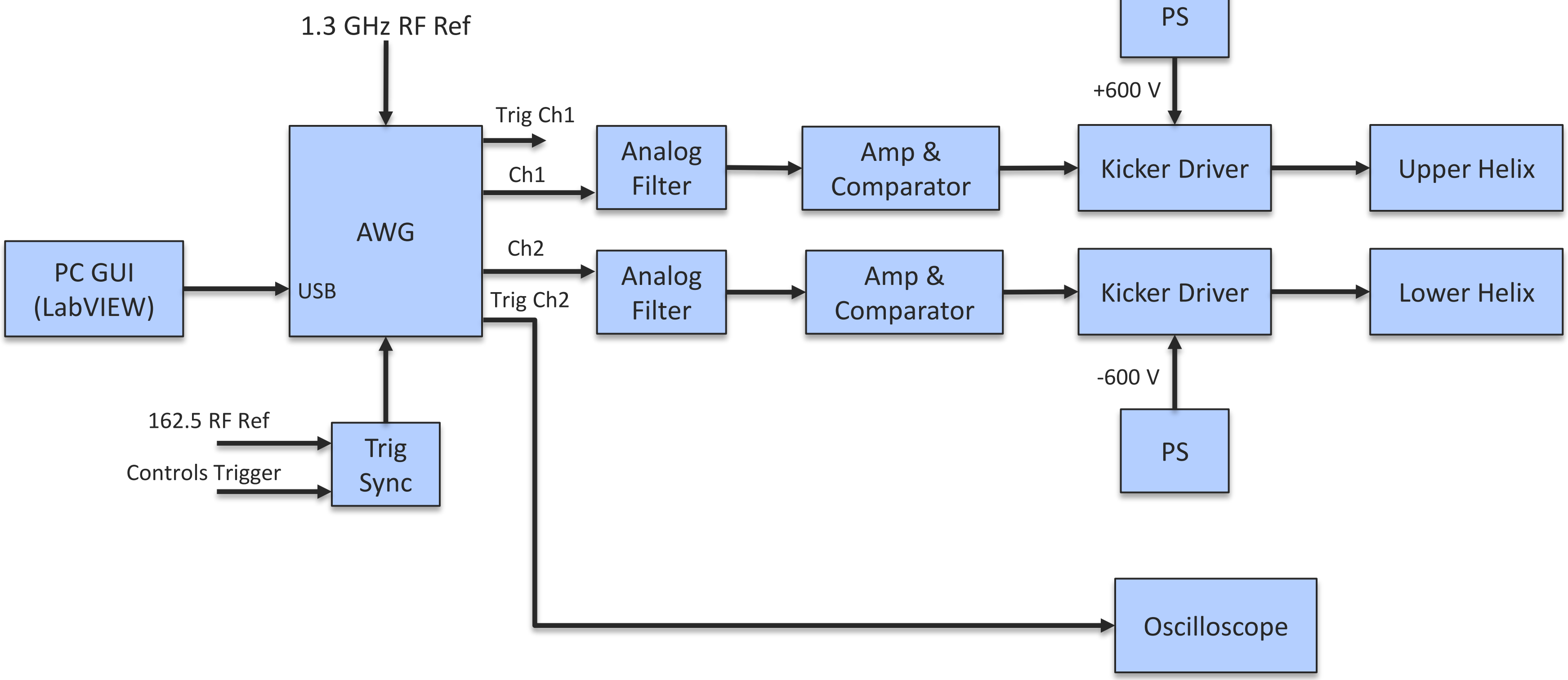


Phase Reference Lines (162.5, 325, 650 ,1300 MHz)



Multi-frequency Phase References and Local Oscillators Being prototyped at BARC

Chopper program generator



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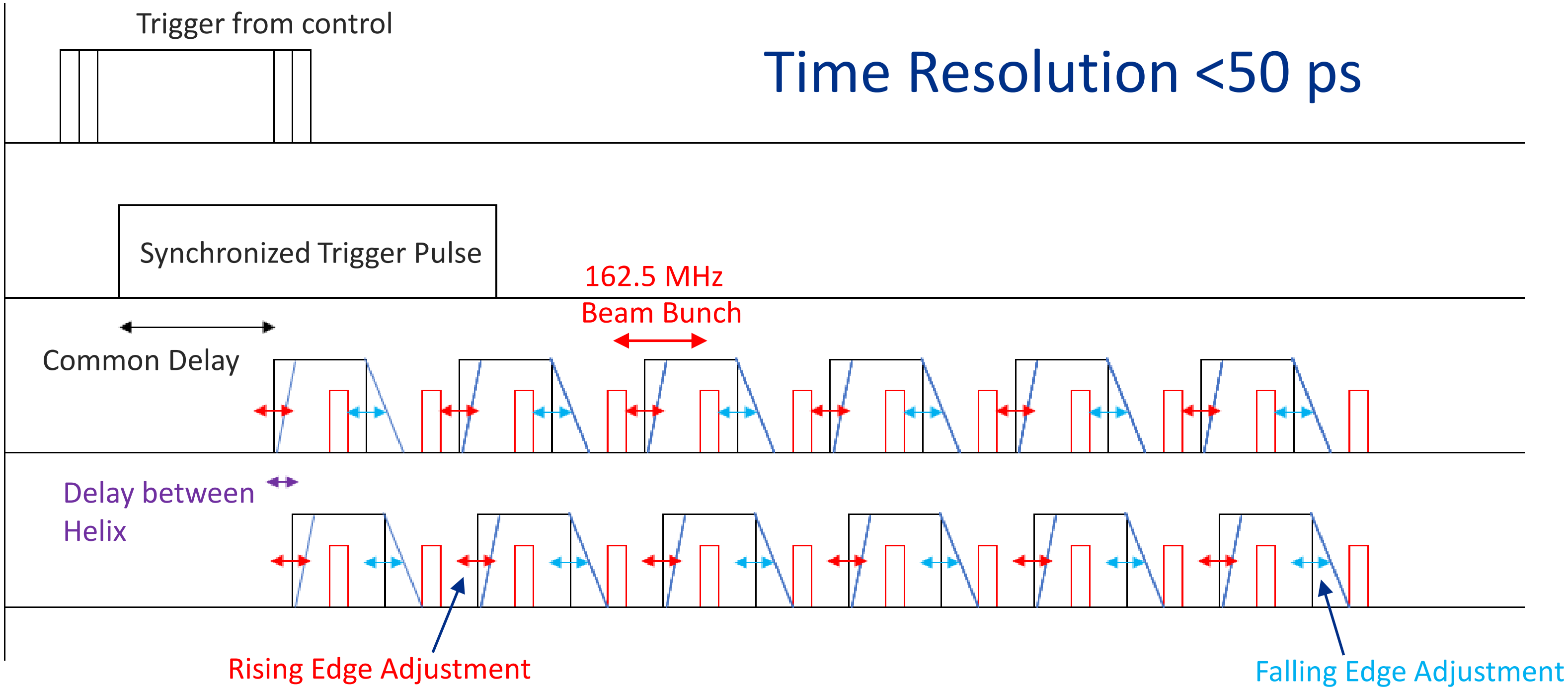


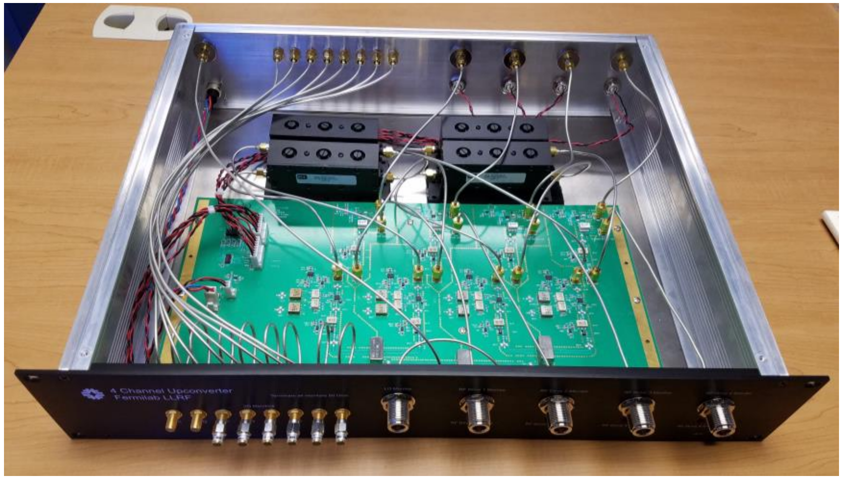
- Delay with respect to synchronized trigger
  - Compensate for cable lengths
  - Compensate for kicker driver delay
  - Internal delay of Arbitrary Waveform Generator (AWG)
- Differential delay
  - Different characteristics of kicker switches

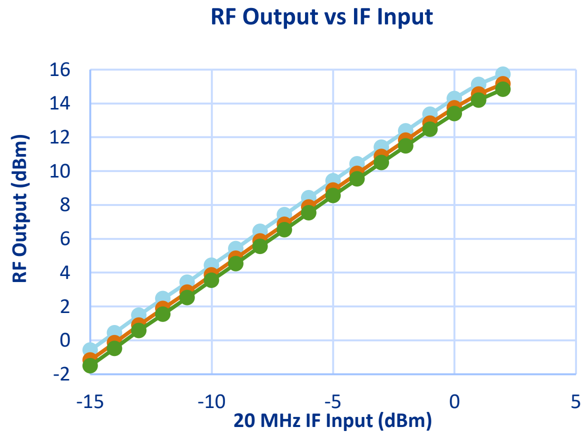
Hardware status to date

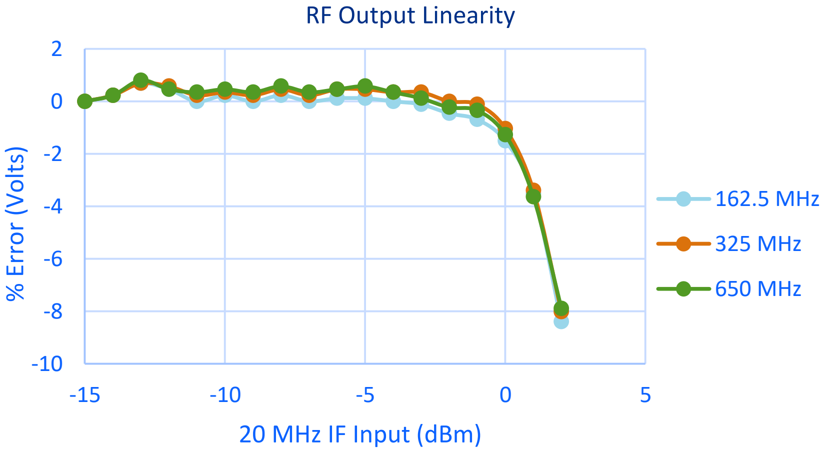
Prototype measurements

4-Channel Up-converter

- 20 MHz IF input -2 dBm max
- 162.5, 325, and 650 MHz Output, +11 dBm max
- 13 dB IF to RF Conversion Gain typ.
- Channel to Channel Isolation > 88 dB
- Spurious Signal Suppression > 80 dB
- High isolation (>68 dB) TTL RF switch
- Power Supply 6V, 1.8 Amp

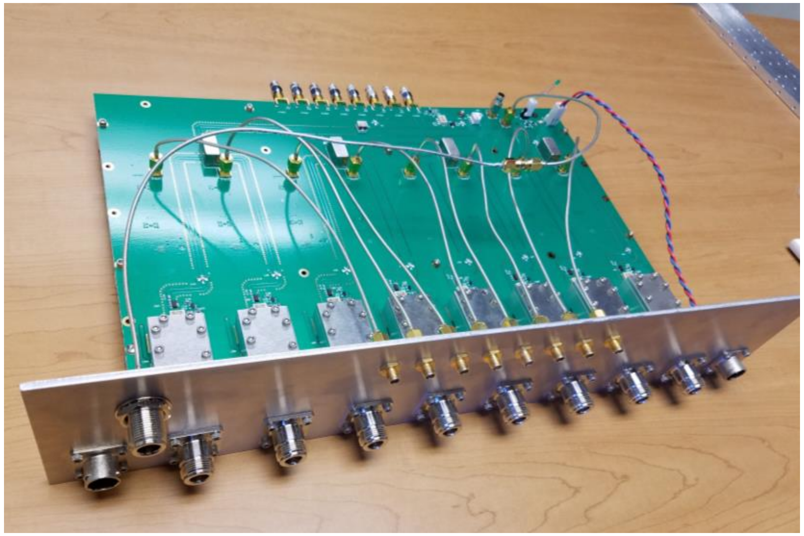


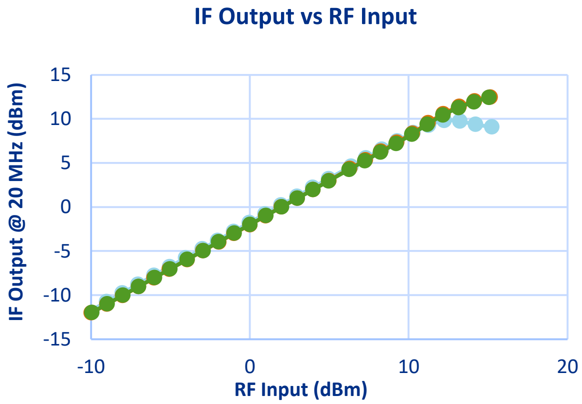


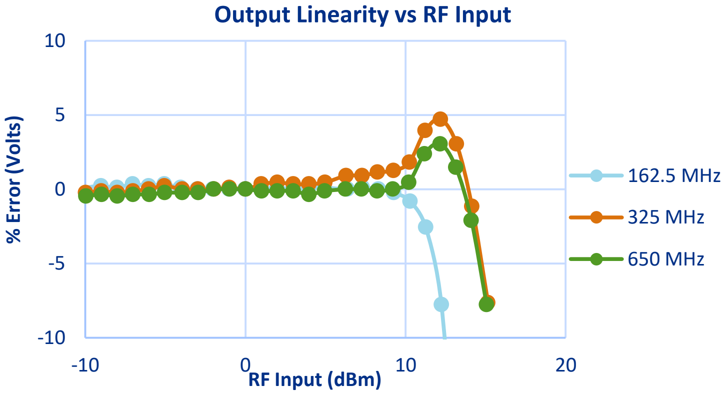


PIP-II LLRF 8-Channel Downconverter Prototype

- RF input 162.5 MHz – 650 MHz
- Less than 1% non-linearity up to 10 dBm RF input
- 1.8, 2.1, 2 dB conversion loss @ 162.5, 325, 650 MHz respectively
- Better than 82 dB Channel to Channel Isolation
- RF, LO, IF monitor ports
- Absorptive IF output low pass filter
- Noise output floor of -161 dBc/sqrt(Hz)
- Integrated output 1/f noise < 1.84 fsec, (0.02 to 20 Hz)
- LO Input power of 3.1, 3.8, and 5.7 dBm @ 162.5, 325, 650 MHz respectively
- Power Supply 6V, 2.25 Amps



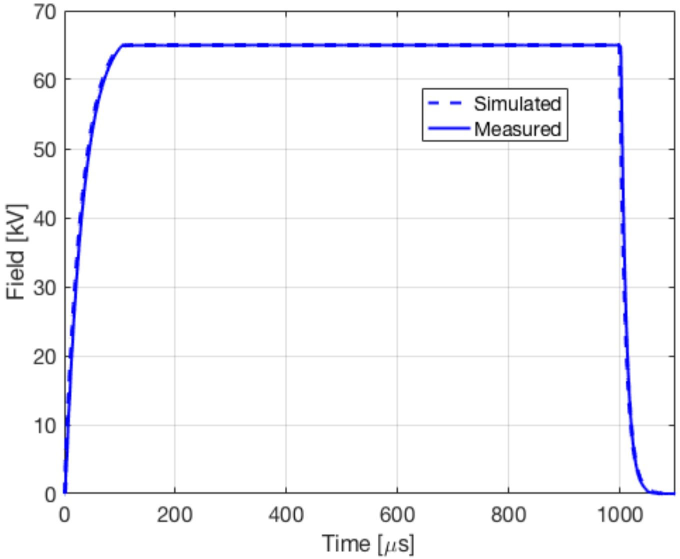


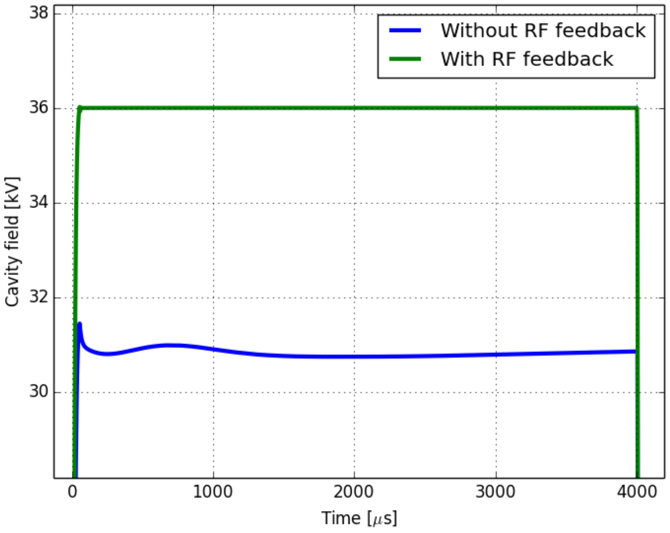


Fermilab

Measurements from PIP-II injector test

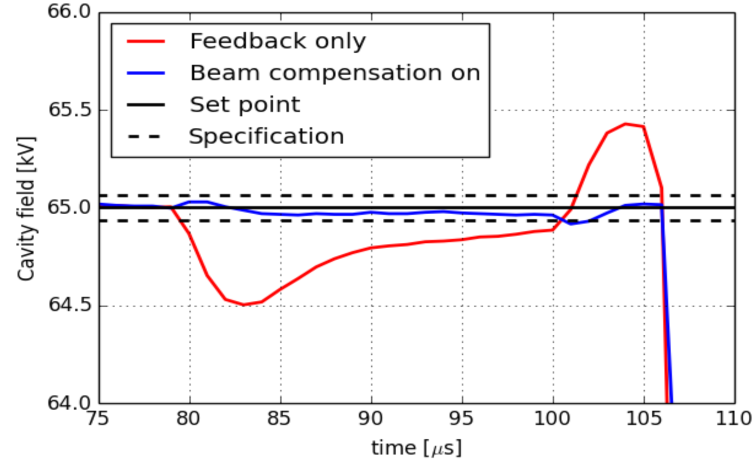
- To date we have operational experience with the RFQ and three bunching cavities
- Left: Models of the RFQ LLRF system match well with measurements
- Right: Phase and amplitude ripple on the amplifiers complicate frequency tracking mode (modified frequency tracking loop for copper cavities)

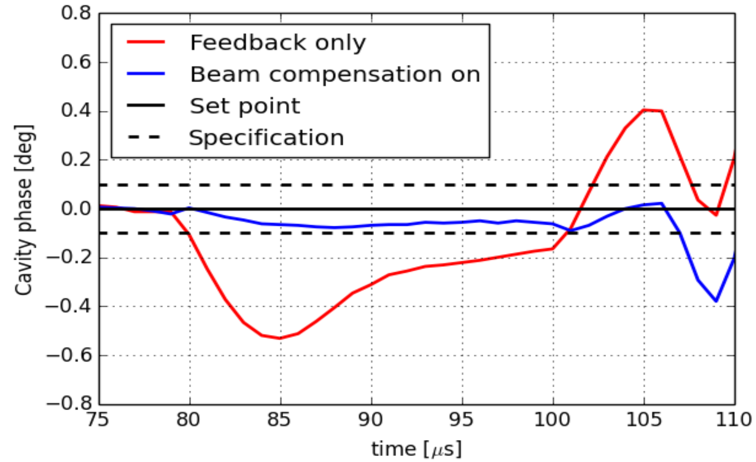


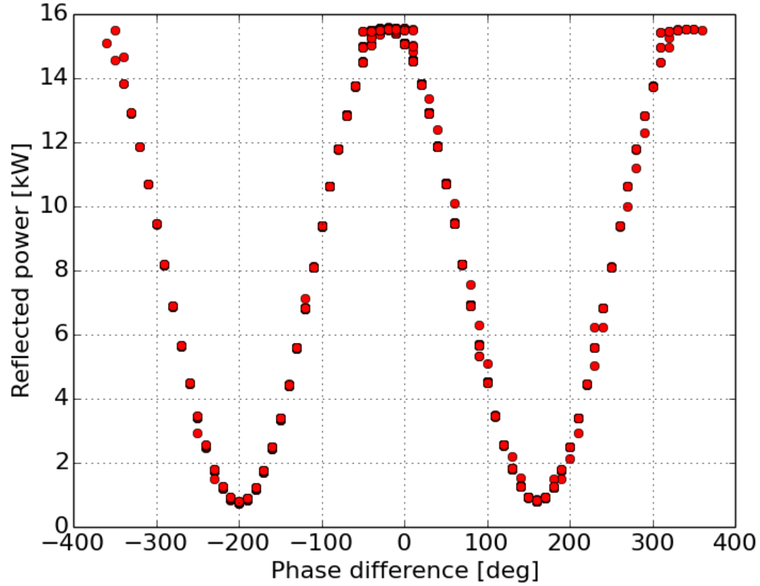


Measurements from PIP-II injector test

- Feed-forward is used to reduce the beam-loading transient in the RFQ
- Initial specification of 10^{-3} is met
- Amplifier phasing is necessary to ensure proper match into the RFQ





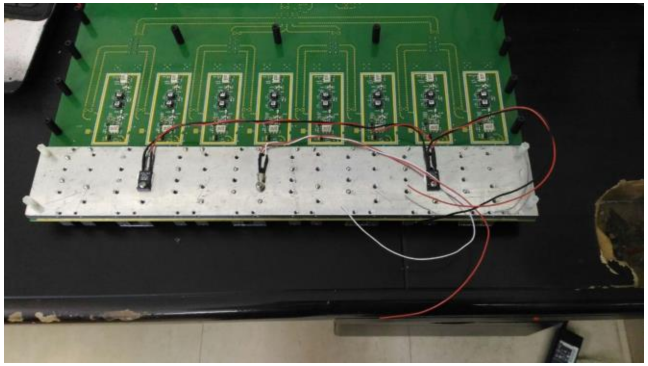


Progress of the IIFC collaboration

- Seven joint FRSs Approved (two more near approval)
  - TRS in process
- 8-Channel Down-Converters
  - BARC version is in manufacturing process
- 4-Channel Up-Converters
  - FNAL version tested
  - BARC version is in manufacturing process
- FPGA Board
  - In schematic review process
- ADC-DAC FMC Module
  - Ready for manufacturing
- Resonance Control Chassis
  - Leverage from FNAL LCLS-II design and is in progress

Up-converter module

Down-converter module



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Conclusions

- PIP-II LLRF design conceptual design is mature and leveraged off of existing designs and past experience
  - Gaining experience from PIP2—IT as well
  - While specifications are tight, simulations indicate we will be able to meet these requirements
  - Our biggest challenge is LFD compensation