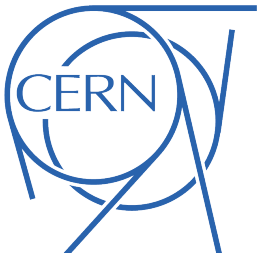
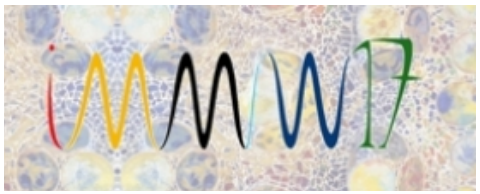


The New Digital Integrator

P. Arpaia[1], B. Celano[1], M. Buzio[2], P. Cimmino[1],
L. Fiscarelli[1,2], C. Giaccio[1], L. Walckiers[2]

[1] University of Sannio, Italy
[2] CERN, Switzerland



IMMW17 La Mola, Terrassa-Barcelona, September 18-23, 2011

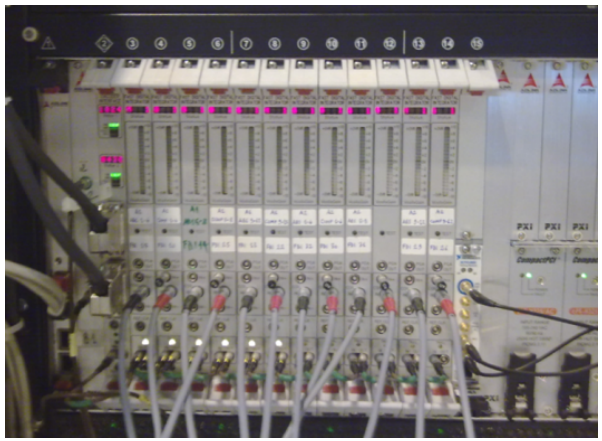
Outline

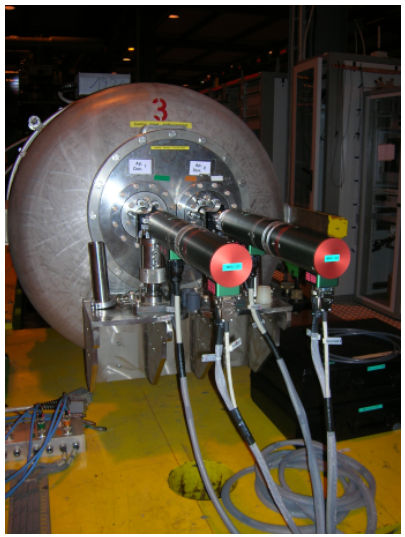
- *Introduction*
- *On-field feedbacks*
- *FDI architecture*
- *New Digital Integrator*
  - *Requirements*
  - *Concept design*
  - *Specific solutions*
- *Conclusions*

FDI at CERN 1/2

Fast Digital Integrator on the field:

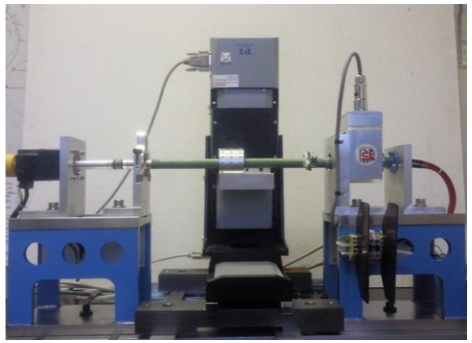
- *LHC dipole test bench (12 FDIs)*
  - *Decay-snapback studies*
- *Magnet prototype bench (6 FDIs)*
  - *Nb_3Sn magnet prototypes*





FDI at CERN 2/2

- *Linac4 bench (3 FDIs)*
  - *Permanent small quadrupole*
  - *Fast-pulsed quadrupole*
- *Magnetic properties bench (1 FDI)*
- *Superconducting cable test (1 FDI)*
  - *Current experiments in cryo-conditions*



On-field feedbacks 1/2

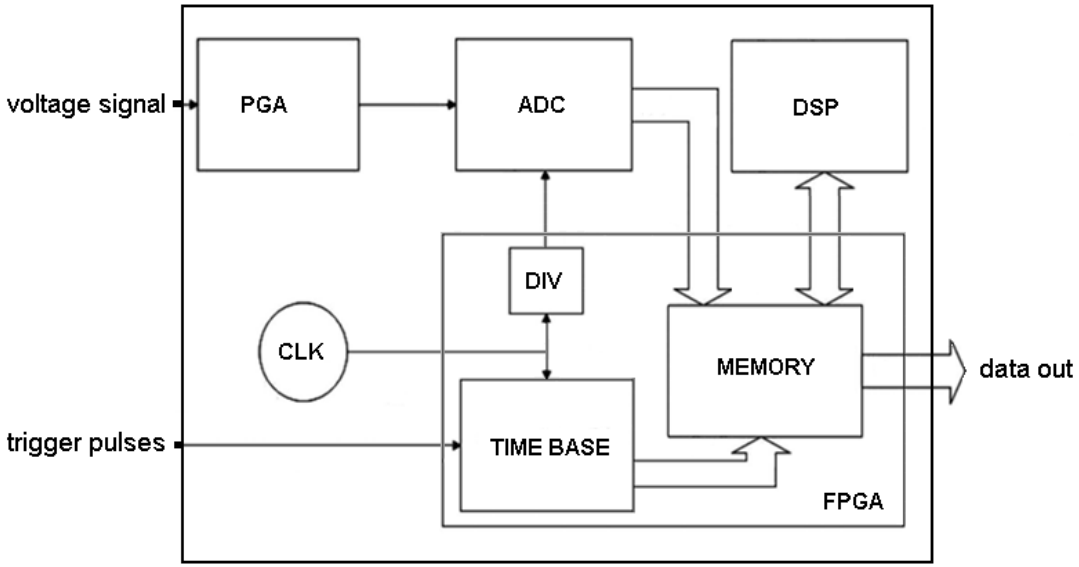
- *Low throughput*
  - *low measurement bandwidth for several FDIs*

- *Lack of on-board memory*
  - *non-optimized data exchange*
  - *no on-line complex algorithms*

On-field feedbacks 2/2

- *Self-calibration ineffectiveness*
  - *residual gain and offset errors*
- *EMC problems of the board*
  - *Noise at high gains*
- *Scarce maintainability of the firmware*
  - *Incremental development of FPGA code*
  - *Difficult upgrade of DSP fw*

FDI architecture



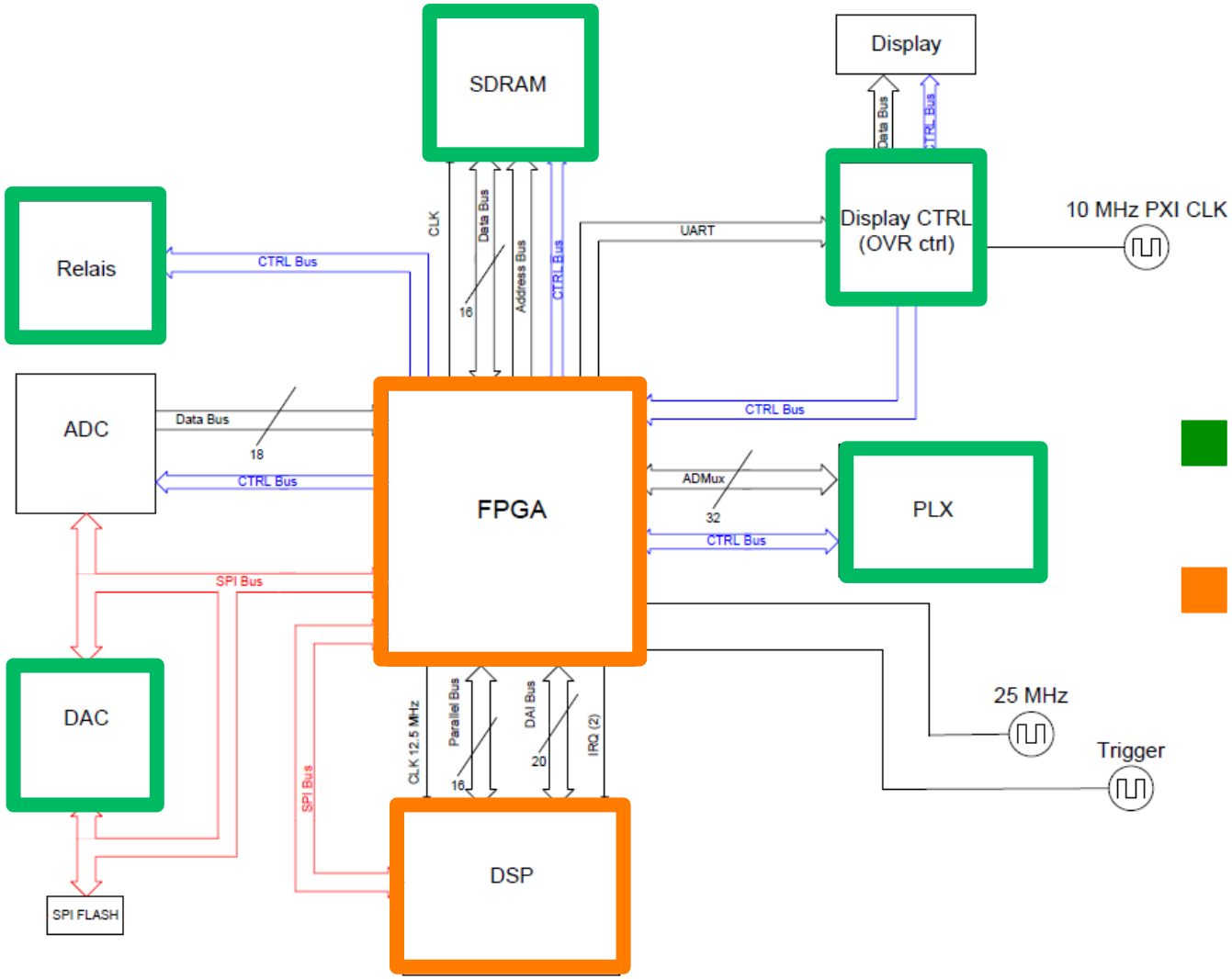
Fast Digital Integrator is based on:

- *High-performance analogue front-end with programmable gain (0.1 to 100)*
- *Fast- and high-resolution ADC (670 kS/s, 18 bit)*
- *High-resolution time base (50 ns)*
- *DSP for integration (trapezoidal rule with interpolation) and other algorithms*
- *FPGA as I/O processor and RAM memory*
- *cPCI interface (6U PXI rack)*

New instrument requirements

- higher throughput
- more memory
- self-calibration upgrade
- optimization of the analogue front-end
- new display and reset management
- re-design of modular code for DSP and FPGA
- remote DSP firmware update from cPCI
- fast gain change

Concept design



New blocks

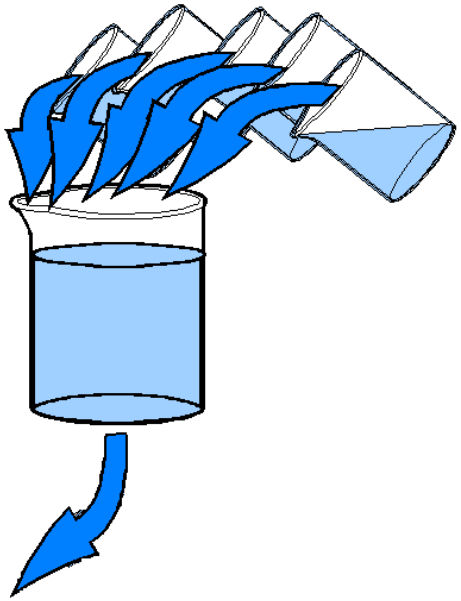
Re-designed blocks

Specific solutions: throughput 1/2

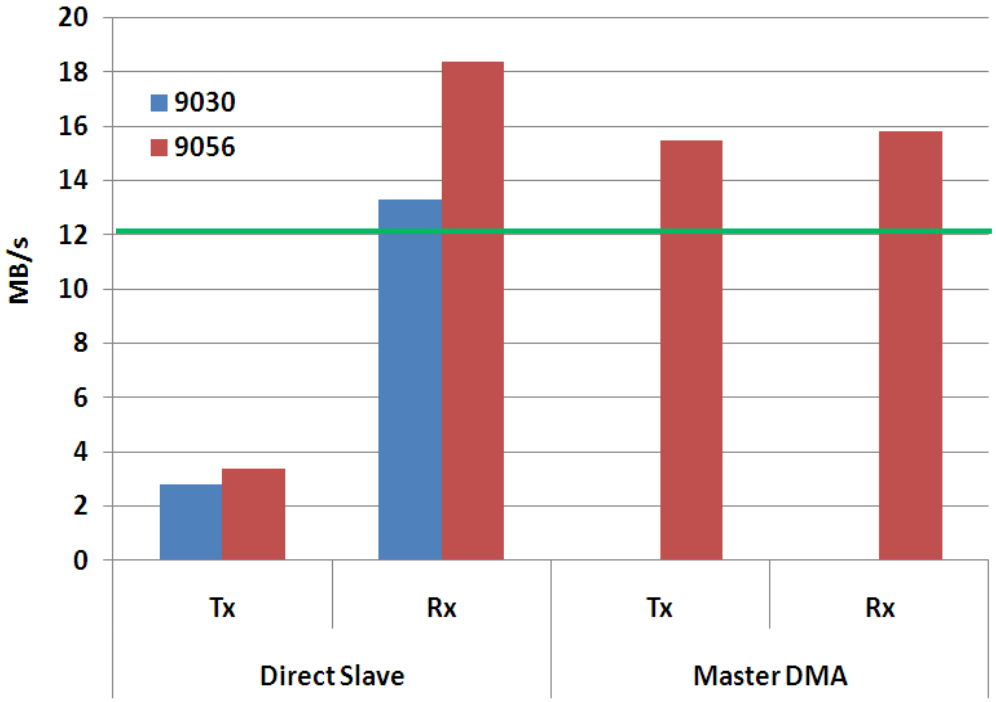
Use case for LHC dipole testing

12 FDI @ 250 kS/s

250 kS/s x 4 B/S x 12 = 12 MB/s



Specific solutions: throughput 2/2



- *Plx PCI9030 (FDI)*
- *Plx PCI9056*

**Average rates measured in actual tests of 1 min, carried out by specific utility included into the PLX driver*

Solution: PCI9056 implementing Master DMA mode

Specific solutions: memory

Optimization of the data exchange requires more memory.

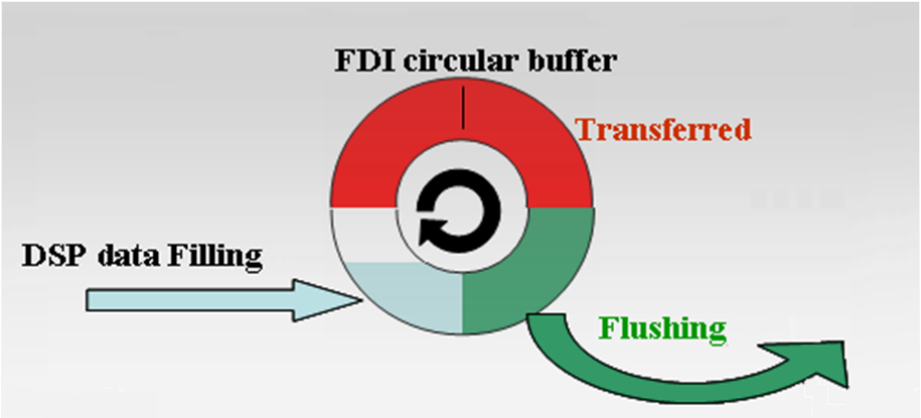
Use case:

1 FDI @ 250 kS/s

1 MB/s

2 MB to store 1 s of acquisition.

Several MB are required.



FDI has only:

- *RAM of the DSP (few kB)*
- *RAM in FPGA (few kB)*

Solution: DRAM module of 16 Mb x 16 x 4 driven by the FPGA.

More complex algorithms (several seconds) can be executed on-board.

Specific solutions: self-calibration 1/2

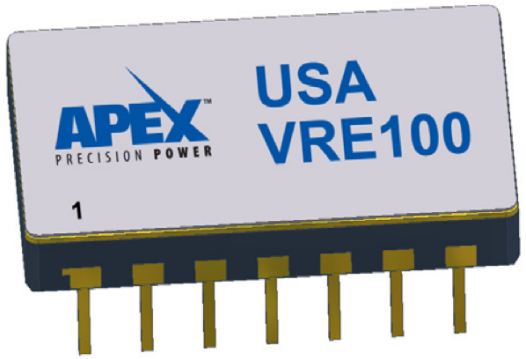
FDI has a high quality ±10 V ref source:

1.09 ppm/°C, 6 ppm/1000 h

The references for the various gains (13 gains from 0.1 to 100) are obtained by

- *dividers*
- *amplifiers*
- *analog mux's*

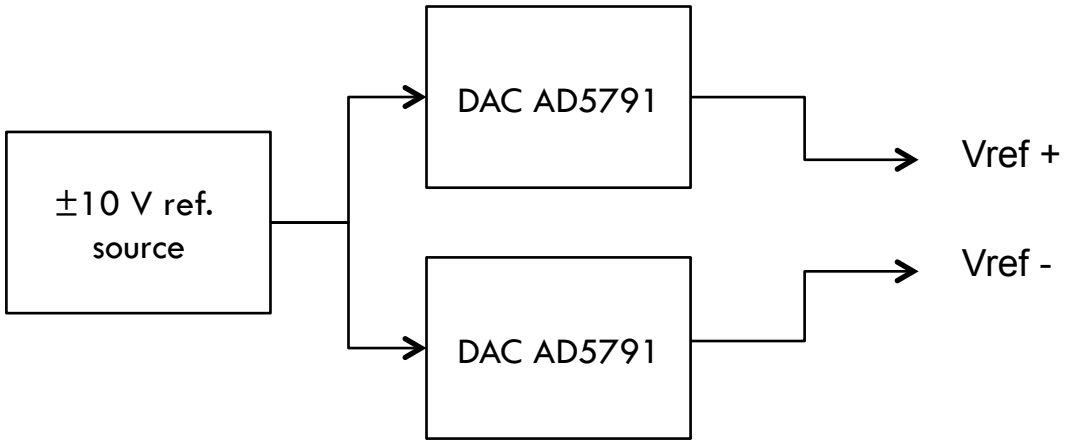
with a significant performance loss (0.1 %)



Specific solutions: self-calibration /2

Solution: instead of dividers/amplifiers, 2 DAC AD5791

- ***20 bits, 1ppm INL***
- ***0.19 LSB long-term linearity***
- ***0.05 ppm/°C***



The availability of a large set of Vref allows to more effective calibration algorithms.

The expected offset and gain errors are in the order of tens of ppm.

Conclusions

FDI has been exploited at CERN intensively.

The physiological development and the feedbacks from field have led to the design of a new instrument.

The new integrator will provide:

- *enhanced throughput to optimize the use of the instrument also in multi-card benches;*
- *on-board memory to manage the data exchange and to allow more complex algorithms;*
- *lower gain errors with more stable voltage reference.*

The first two prototypes are in production now and will be characterized metrologically for the end of 2011.

Thank you

Questions?