Magnetic precision has a name

Fast Digital Integrator Upgrade

IMMW17, J. Tinembart, Sept. 2011

FDI : Brief history

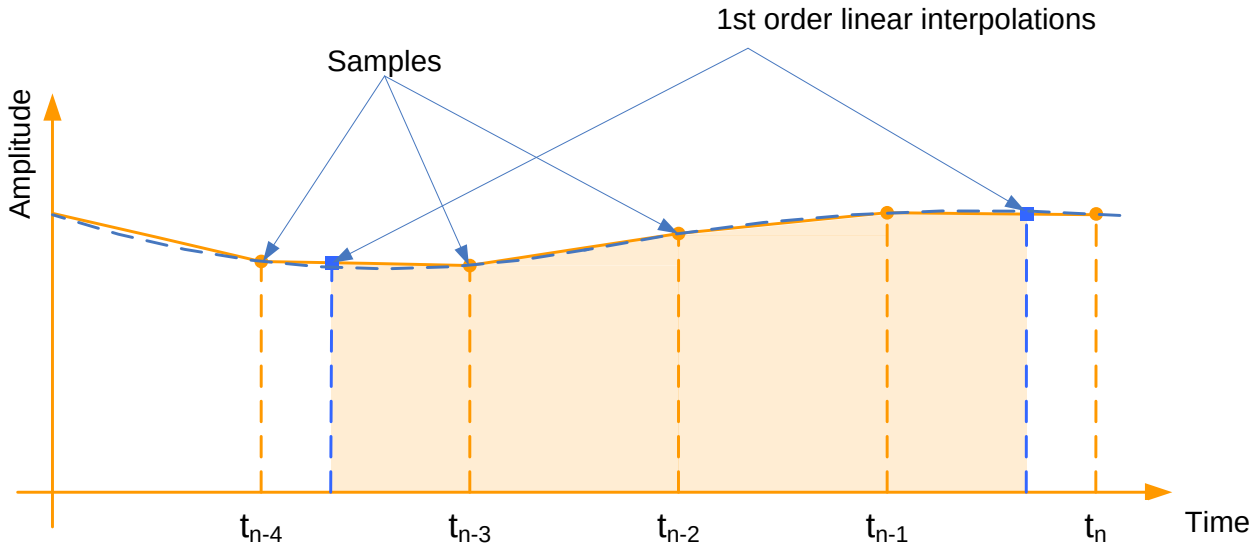
- Designed for LHC superconducting magnet measurement
- Collaborative development by University of Sannio (IT) and various groups at CERN
- License taken by Metrolab to manufacture and sell CERN's FDI in order to provide a successor to "vintage" PDI5025

Why METROLAB chose it

- Performance improvement over PDI5025
- Clever design
- Man-years spent by CERN and University of Sannio
- Many articles and studies, including PHD
  - Full analytical analysis of the noise. (Arpaia et al., IMTC 07)
  - Metrological characterization of a FDI for magnetic measurements at CERN. (Arpaia et al., IMEKO 06)
  - … and more than a dozen more

Principle of integration

- Regularly spaced samples (F_s = 500 kSPS typical, 18-Bit)
- Trigger signal sampled with a time resolution of 50 ns
- Surface is calculated using the amplitude value and trigger position (Trapezoidal Rule)

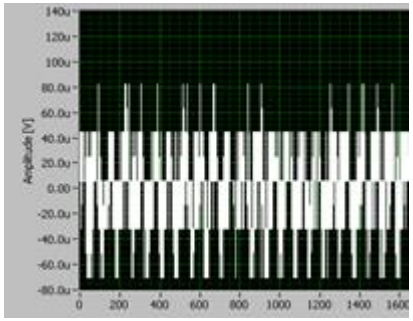


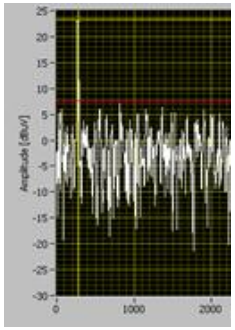
Current limitations

- One trigger input source only
- Visible time lag when boards are daisy-chained
- Poll-only data transfer mechanism
- 2^n trigger counts, resulting in 2^n-1 partial integrals
- Trigger time resolution limited to 50 ns
- Trigger rate > 100 kPI/s cannot be achieved simply
- Cannot work as a simple acquisition board
- Not field-upgradable

Current problems (I)

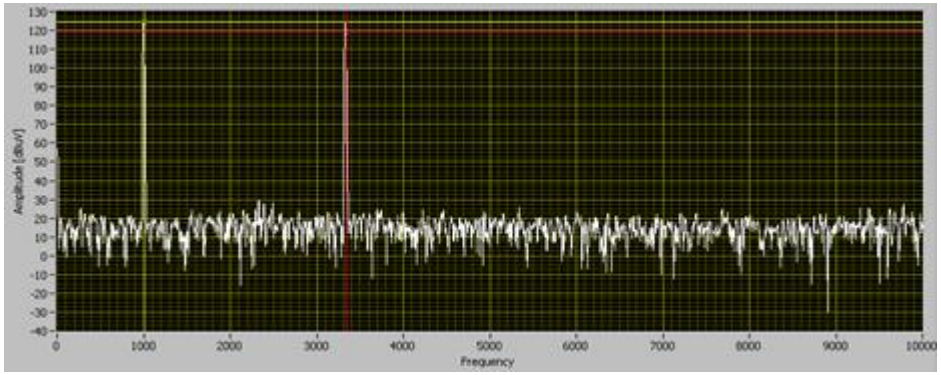
- Defaults that can be corrected :
  - Multiple quartz sources on the board => generates beatings





(Time- and frequency-domain noise measurement)

  - Protection diode at the input => non linearity



(Two-tone signal without protection diode)

Current problems (II)

- Defaults that cannot be corrected :
  - Input is not floating
  - Not fully EMC compliant
- Restrictions :
  - Input impedance is non negligible
  - Coil impedance not taken into account when performing internal normalization
  - Maximum gain is 100x, but this is justified
  - 1-1.2 MB/s transfer rate
    (onboard memory could limit this problem)

Customer feedback

- Reported bugs :
  - Strange saw-tooth pattern (not fully explained)
  - Integration value changes with sampling rate
  - Fast trigger generation leads to calculation error
  - Buffer overflow error reporting is non functional

- The board design is a **good basis** but needs improvement

Revised FDI “wish-list” (I)

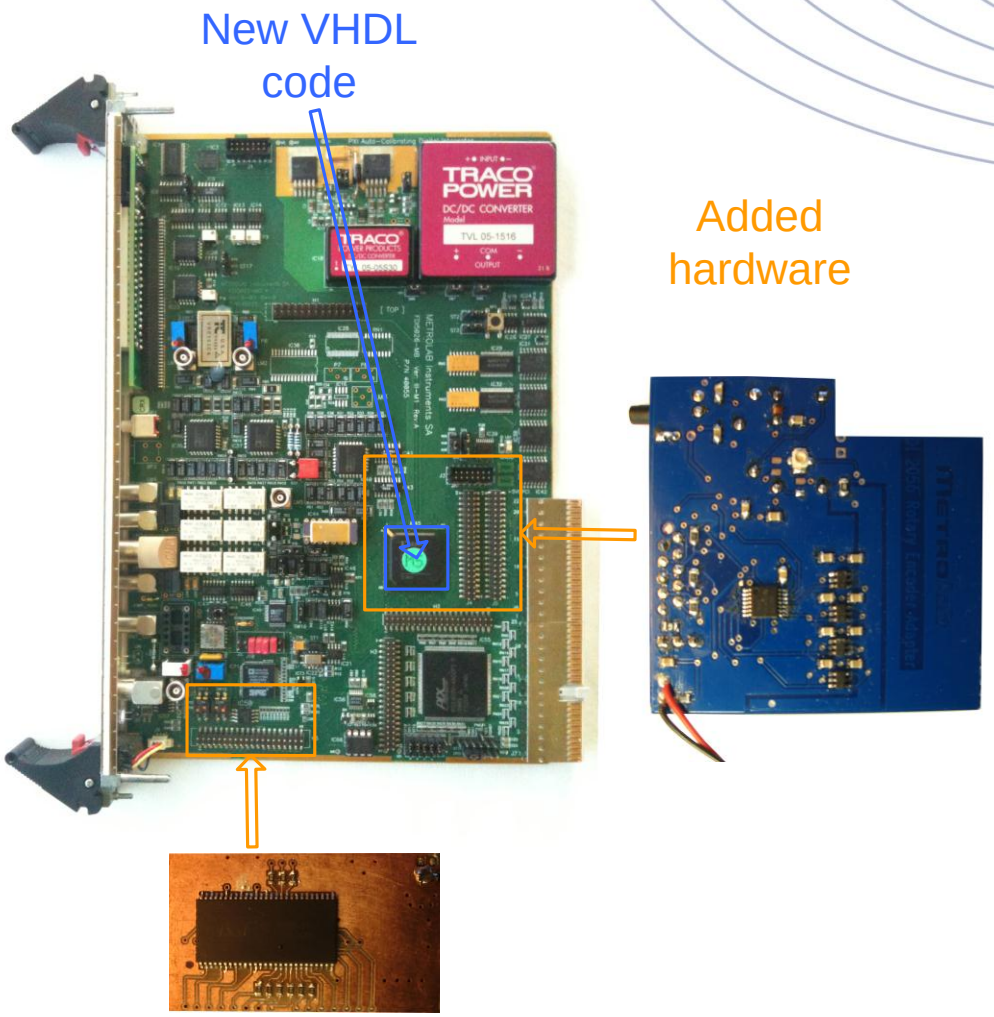
- Quadrature signal decoder :
  - Linear or rotating encoder, with or without index
  - Read-out of current pulse count
  - Missing pulse detection
- Trigger Factory :
  - External trigger
  - Timed trigger
  - Quadrature signal decoder trigger
  - Software trigger
  - Simultaneous multichannel trigger

Revised FDI “wish-list” (II)

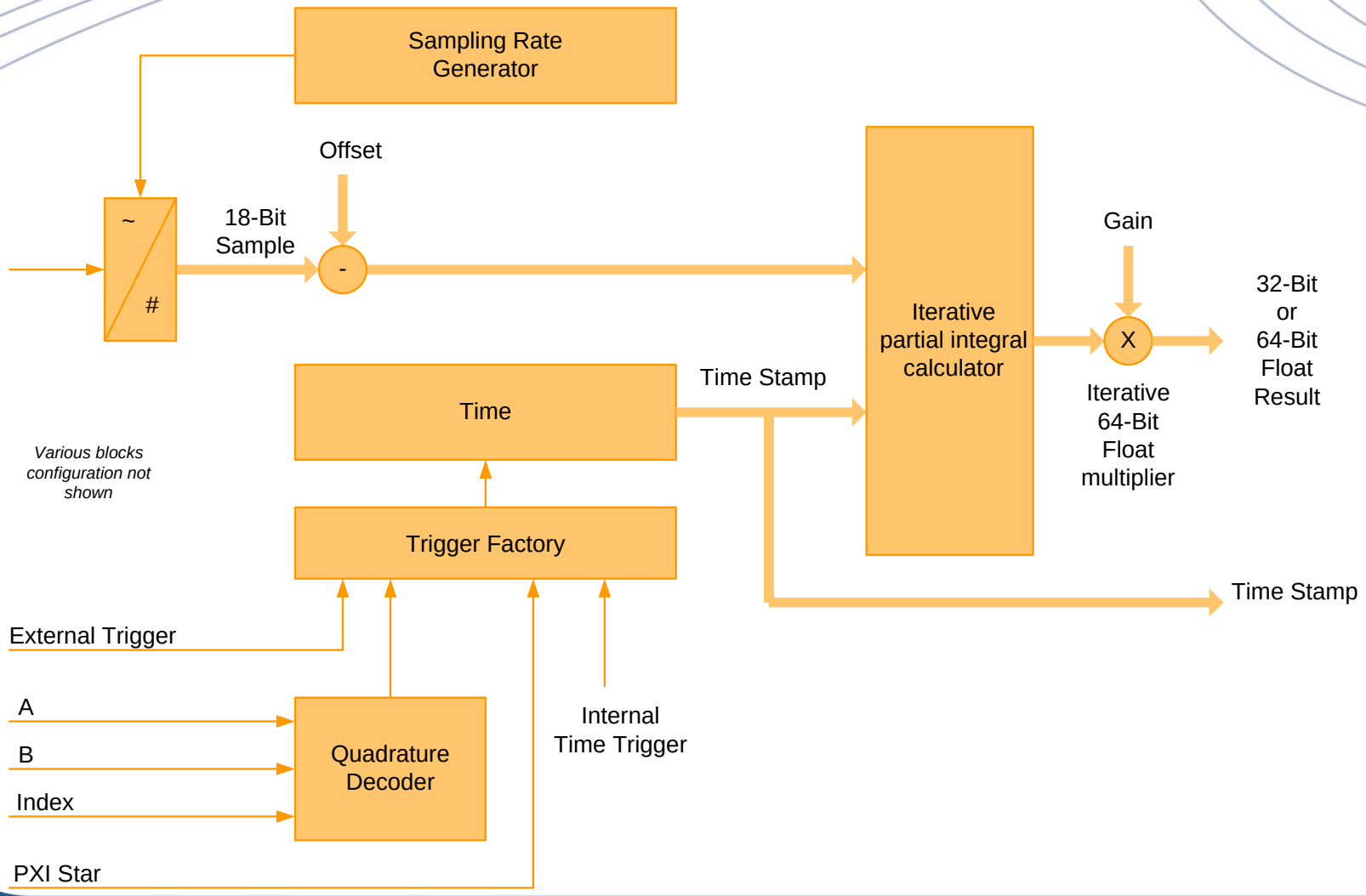
- Sampler mode (Voltmeter)
- Higher trigger time resolution
- Single reference clock for all channels
- Interrupt for data transfer and error handling
- Field upgradable
- Onboard memory
- Higher integration rate (670 kPI/s)

Aim for simplicity

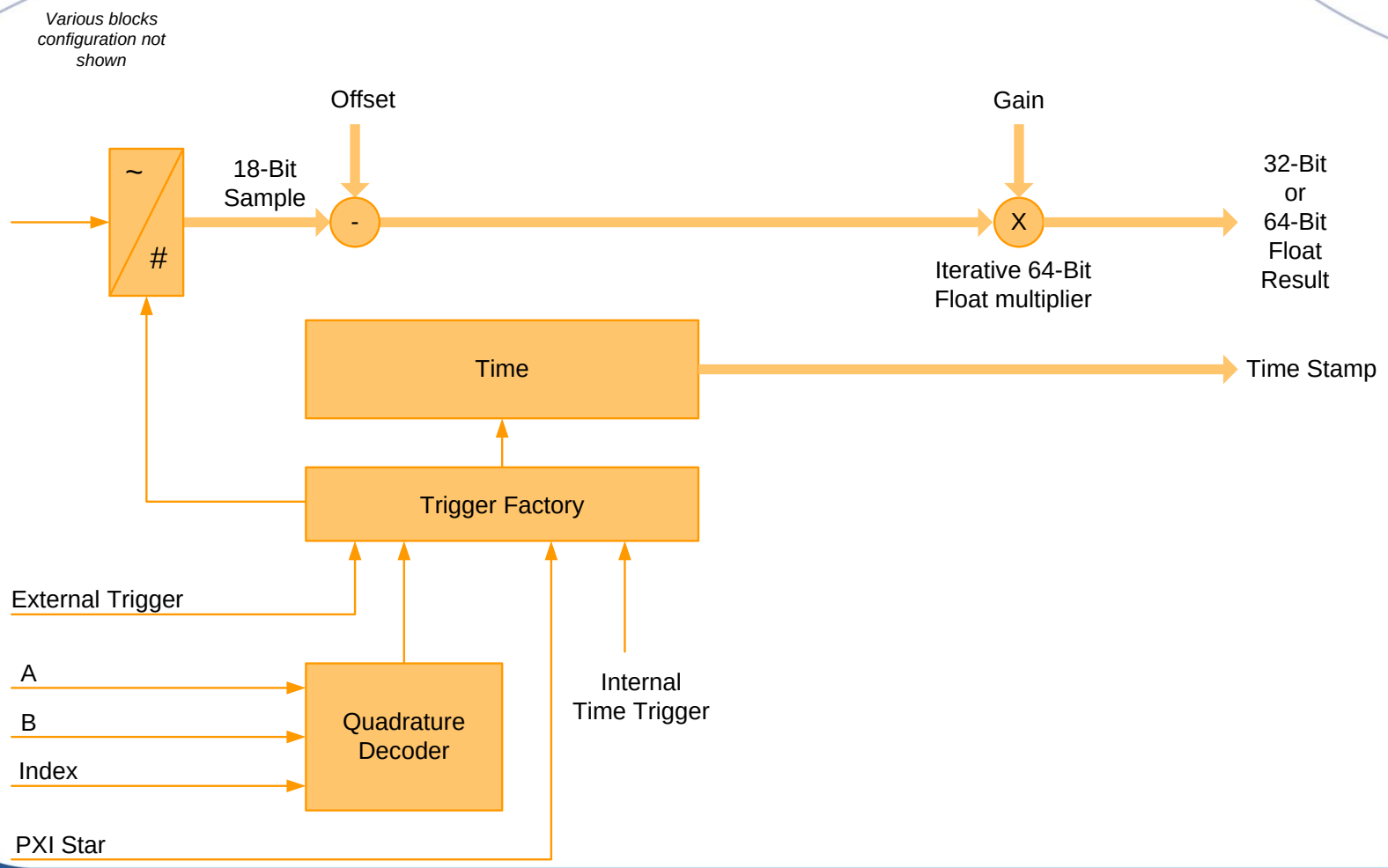
- Minimal changes :
  - SDRAM chip
  - Drivers for encoder
  - Fuse ! (rearmable !!)
  - DSP not used for integration
  - **Reworked VHDL code for FPGA**
- Keeping in mind that all sold units will have to be retrofitted !!!



Block diagram : Integrator

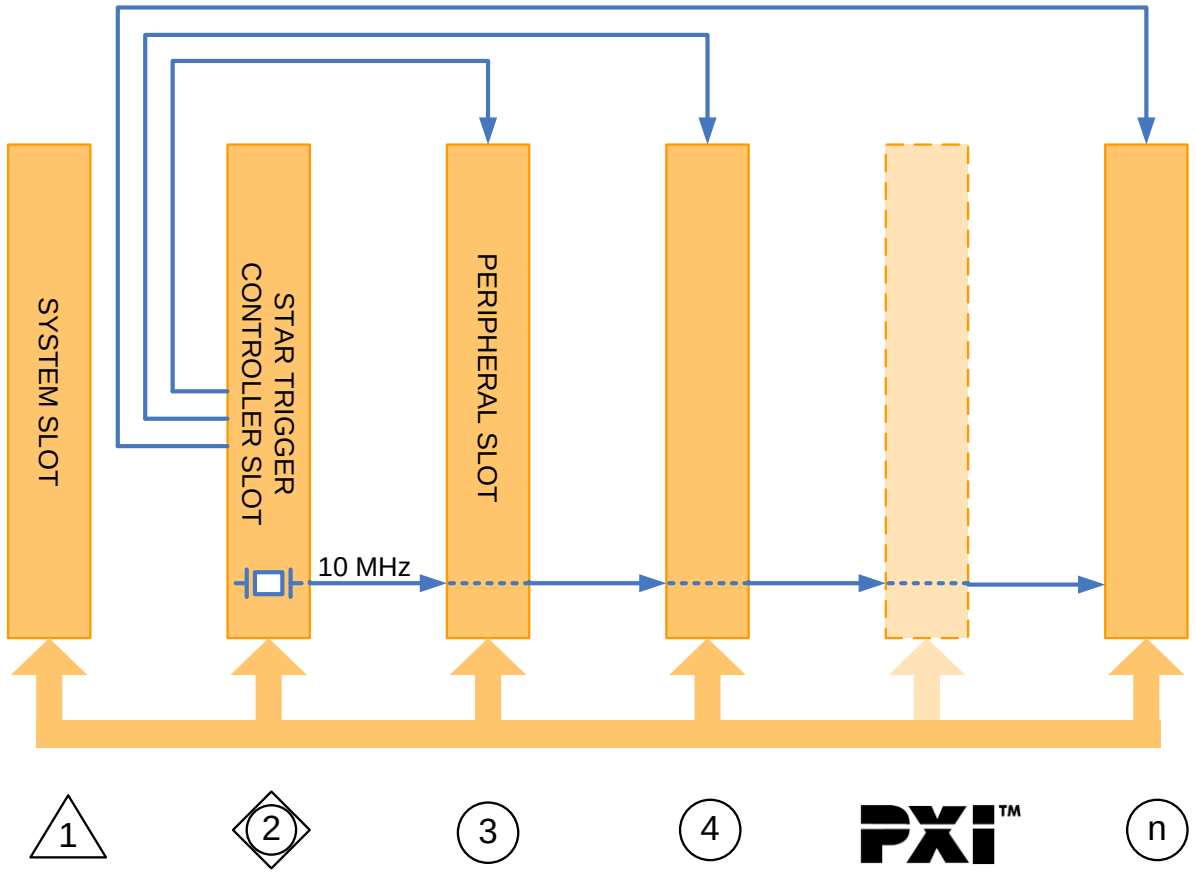


Block diagram : Sampler



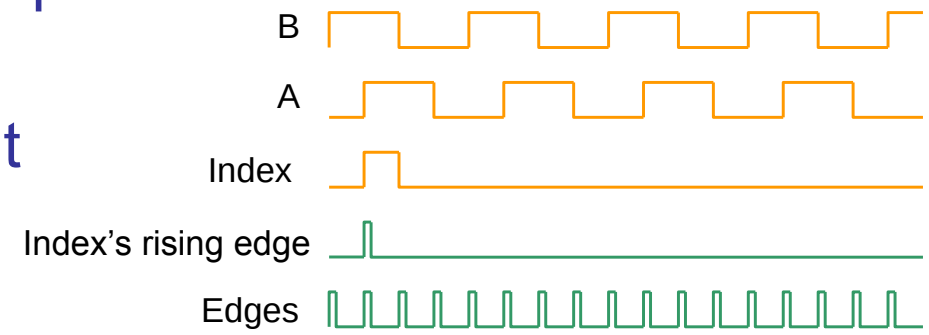
PXI Star Trigger and clocking

RULE: The PXI_STAR line lengths SHALL be matched in propagation delay to within 1 ns, and the delay from the star trigger slot to each peripheral module SHALL NOT exceed 5 ns.



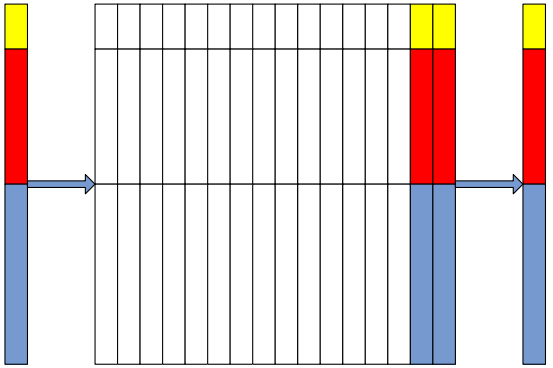
Quadrature signal decoder

- Decode linear or rotary quadrature signals
  - A, B, Index and Error input
  - Single-ended or differential
  - Each input can be inverted by software
  - Internal 90° index is reconstructed
- Works with indexed or non-indexed units
- Keeps track of the current position
- Alarm fires when index position isn't at zero count



Trigger Factory

- Based on configuration word consisting of a
  - Trigger Source
  - Pre-scale Value
  - Count Value
- 16-word configuration FIFO
  - A new word is read after Count Value is exhausted
  - Each exhausted word leaves room to a new word



- Acquisition is done when FIFO is exhausted

Example: acquisition for multi-pole analysis

Acquisition of 555 partial integrals starting 12° after index, using a 1024-line encoder :

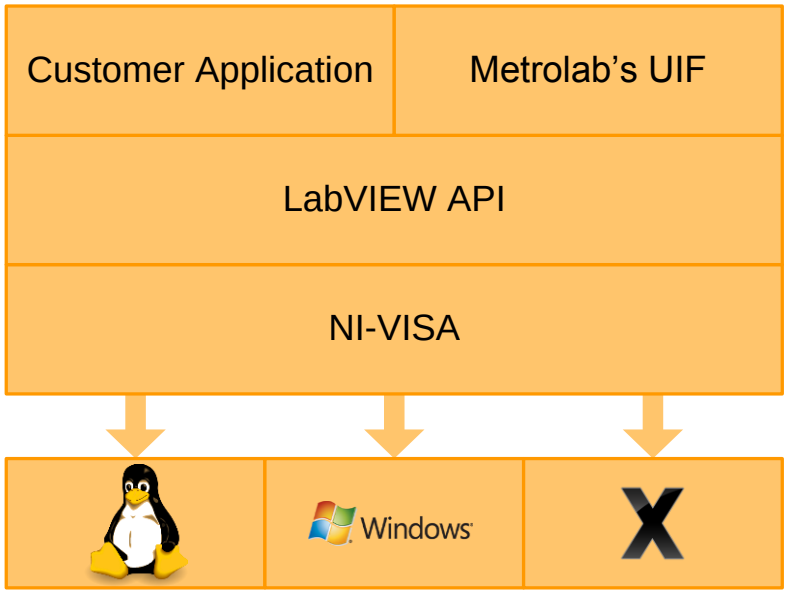
- 2 configuration words are used :

Trigger source	Prescale value	Count value
Encoder position	1	1
Encoder edge	4	555

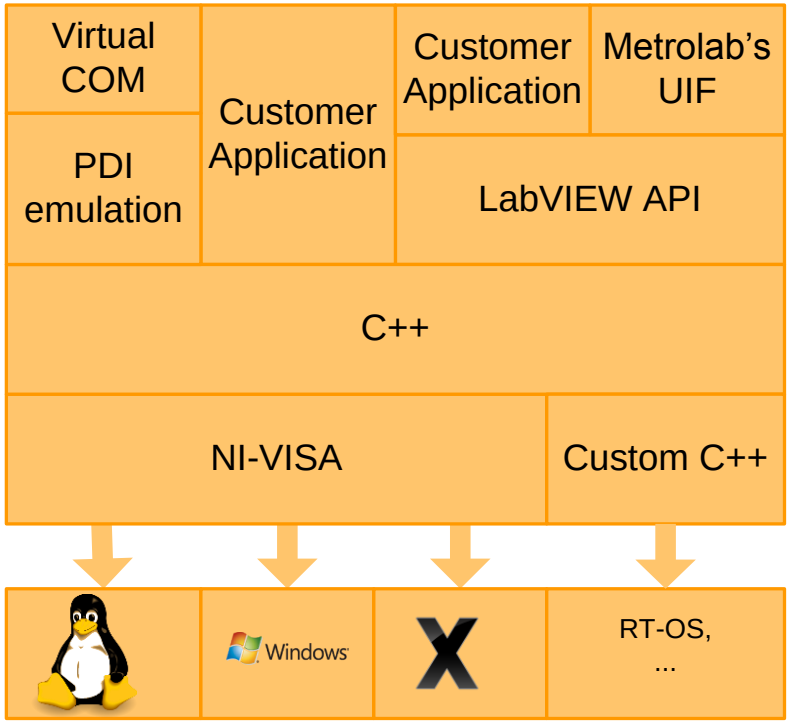
- Acquisition start at absolute position, limited by the encoder : 136/4096*360° = 11.95°
- Encoder position must be written in another register, part of quadrature decoder

Software driver / interface

- Current software layers



- Future software layers



Brief integrator comparison

	PDI5025	FDI2056	FDI2056 (revised)
Trigger rate	1 kI/s	250 kPI/s	Up to 670 kPI/s
Time resolution	2 µs	50 ns	8.33 ns
Data transfer rate	1 KB/s	1 MB/s	1 MB/s
Internal data storage	5200 values	16 x 32-Bit words	At least 8 MB
Trigger Factory	Internal	External	Internal
Channel synchronization	Internal (2 channels)	External	Internal (Up to 12 channels)

Thanks for your attention !

QUESTIONs ? (or tapas)