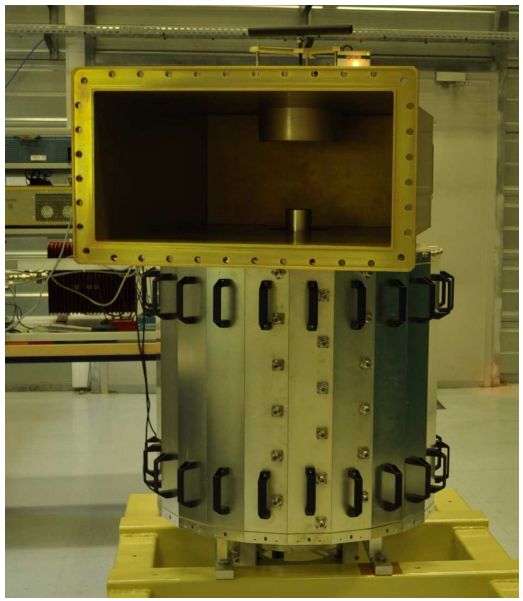
Development of solid state amplifiers at ESRF



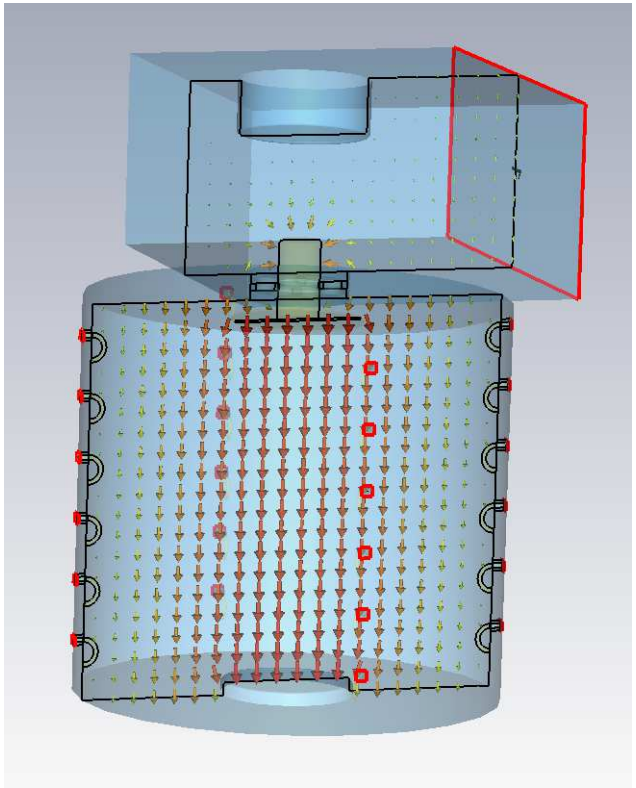
Cavity combiner prototype

Michel Langlois

** This work, carried out within the framework of the CRISP project, has received research funding from the EU Seventh Framework Programme, FP7.*

RF combining : the cavity combiner

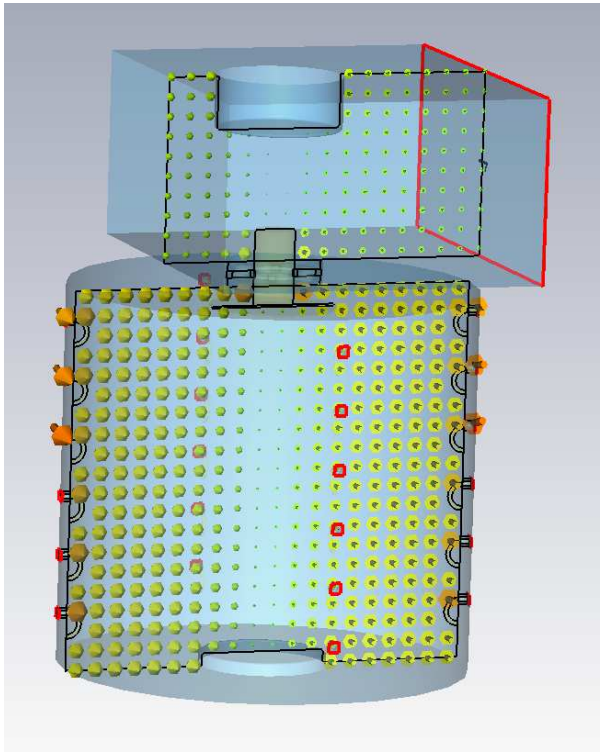
We developed a cavity combiner which could couple up to 132 RF modules. Input coupling is provided by loops on the periphery. Output coupling is capacitive and excite the fundamental rectangular waveguide mode.



E field

E010 mode

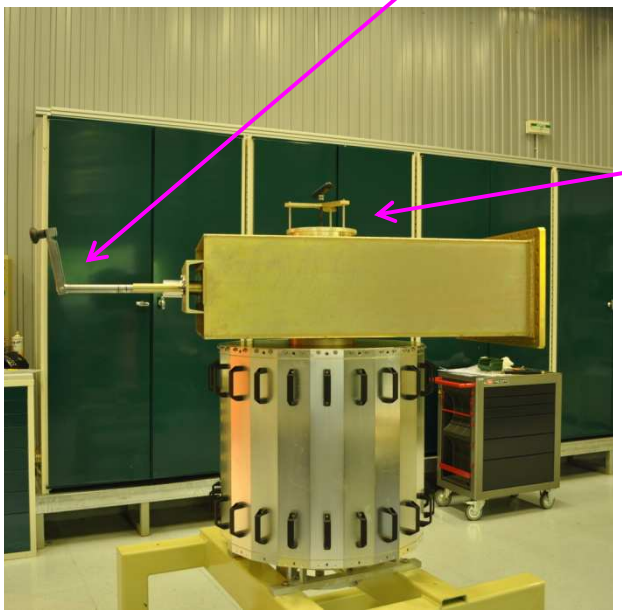
Note: a coaxial output is possible



H field

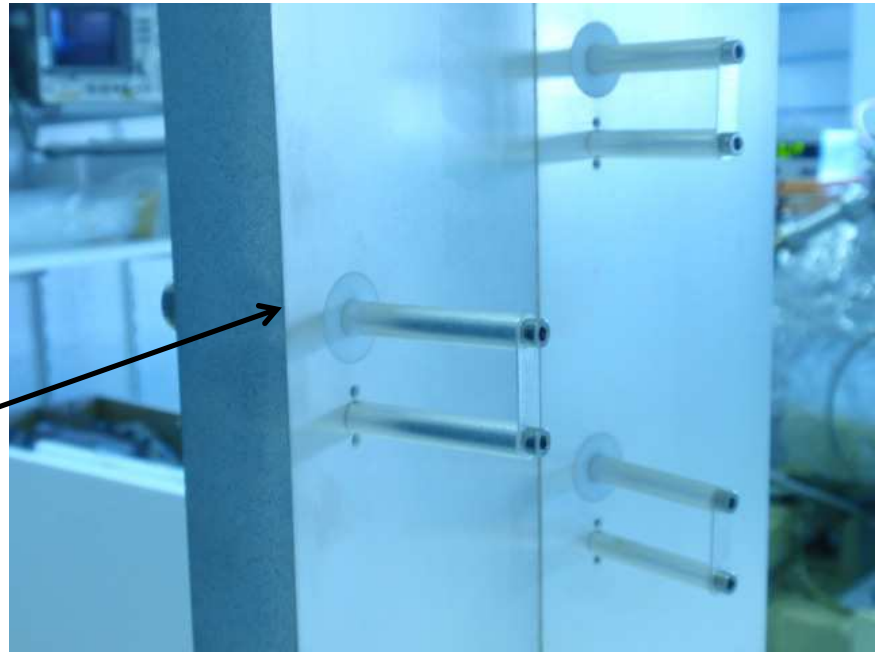
Cavity combiner: the prototype

The waveguide short-circuit can be moved



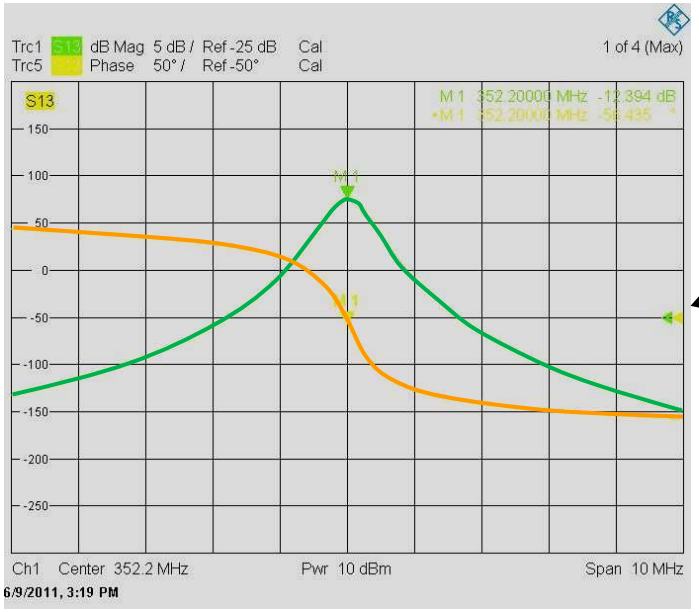
Coupling to the capacitive post can be trimmed

input coupling seen from inside



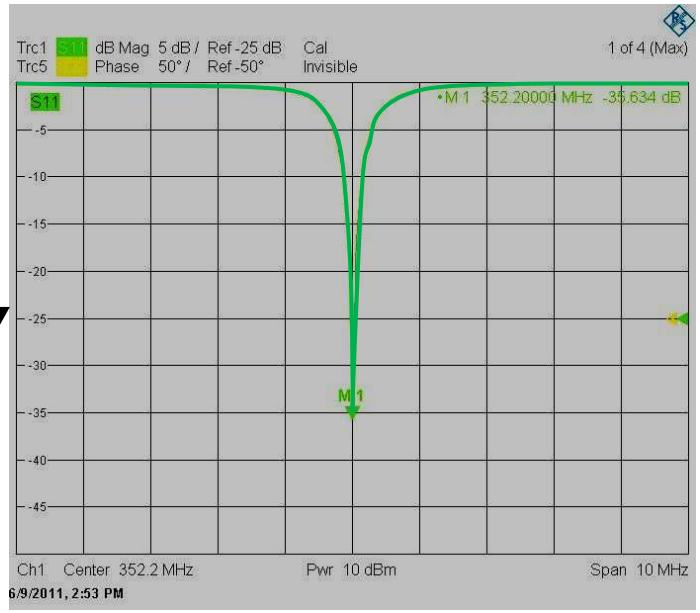
The width and the height of the loops can be adjusted.

cavity combiner: low level results



S31 plot measured with a NWA
1 being the waveguide output port

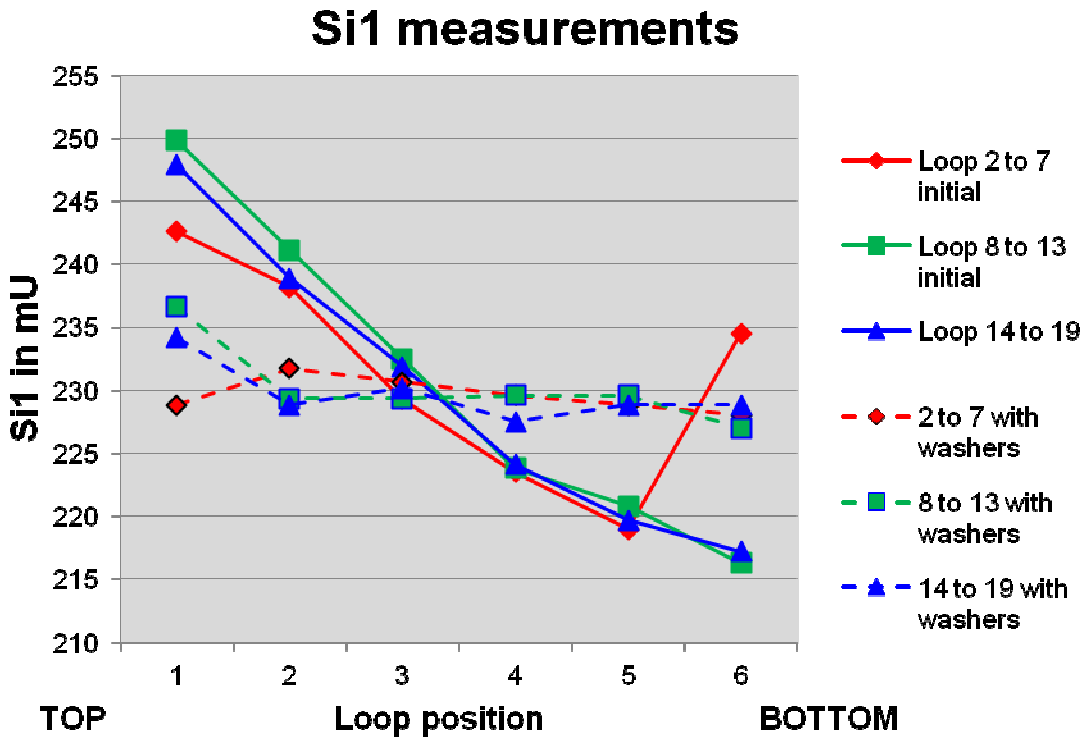
S11 plot measured with a NWA.
The output can be matched with 7 to 18 inputs without changing the loop size.



Cavity combiner: issues

- The behaviour with power has not yet been tested.
- There is a discrepancy on S1i, depending on the i loop position. The loop size must vary with position.

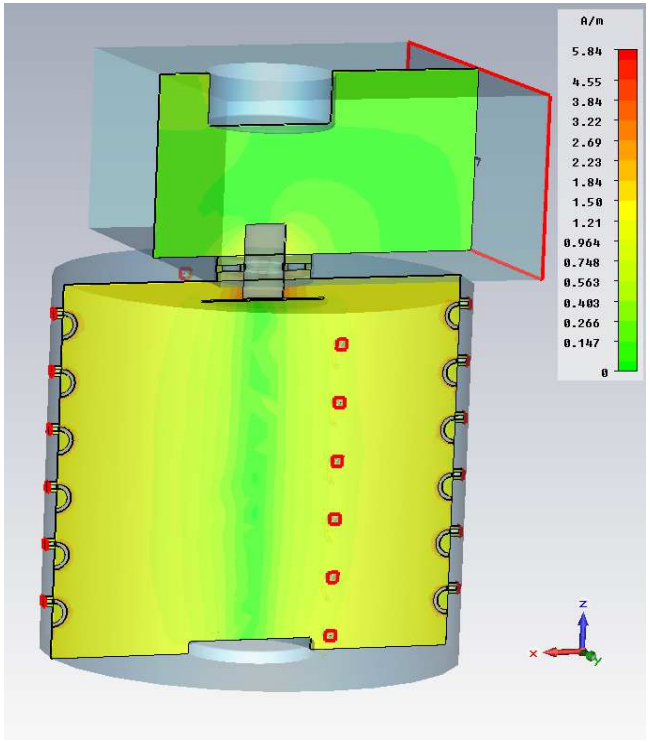
We adjusted washers on the loops to vary their heights and got close values for all S_{i1}



The cavity combiner : losses

Theory:

Most of the losses are due to the current in the cylindrical wall.
We computed 1.35 kW for 75 kW output (conductivity:$5*10^7$ S/m). It does not depend heavily on the number of input loops. It means 0.08 dB insertion loss.

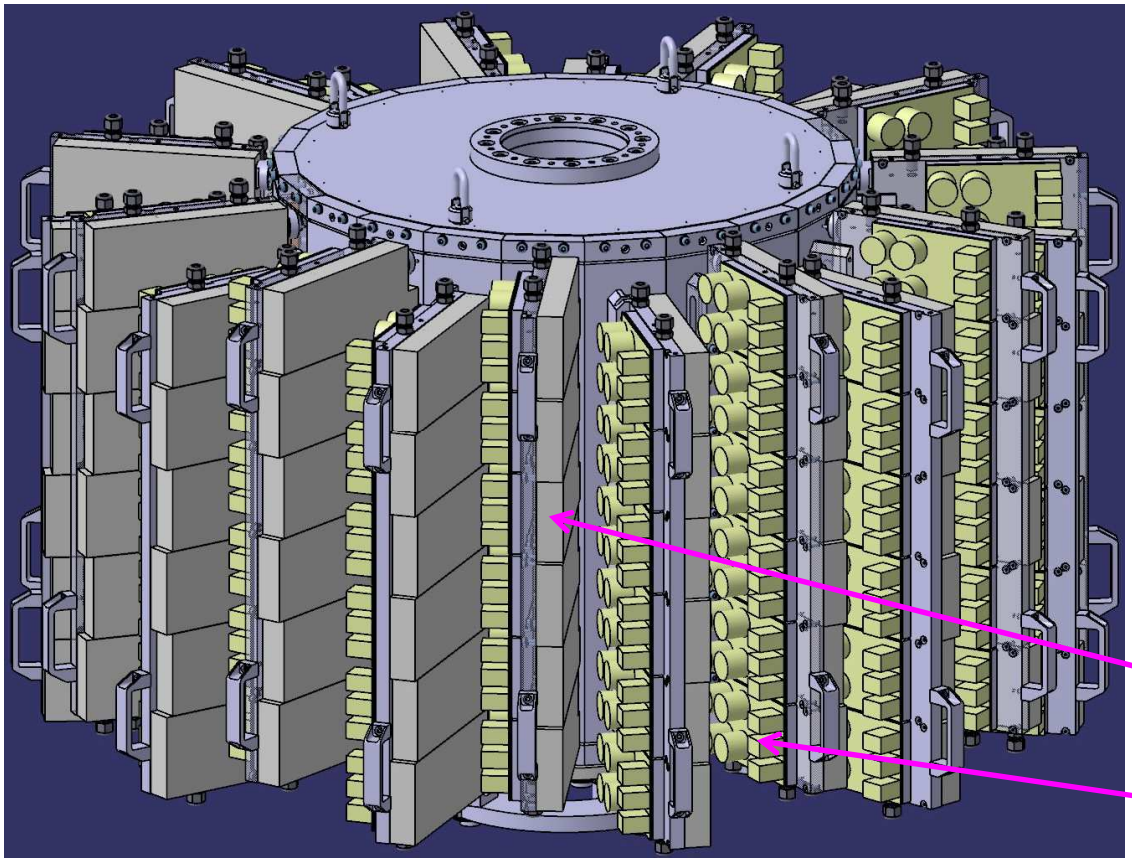


Low level measurements:

$$\left|\sum_{i=2}^{19} S_{i,1}\right| = \sqrt{17.23}$$

The theoretical value would be $\sqrt{18}$
A dubious contact was seen on the movable short circuit, but straightening the waveguide sagging did not change $\Sigma S_{1,i}$.

cavity combiner: modules implementation



The cavity is made of 22 columns bearing 6 RF modules each. On this picture, the AC/DC converters are located on the same cooling plate. This option is no longer considered.

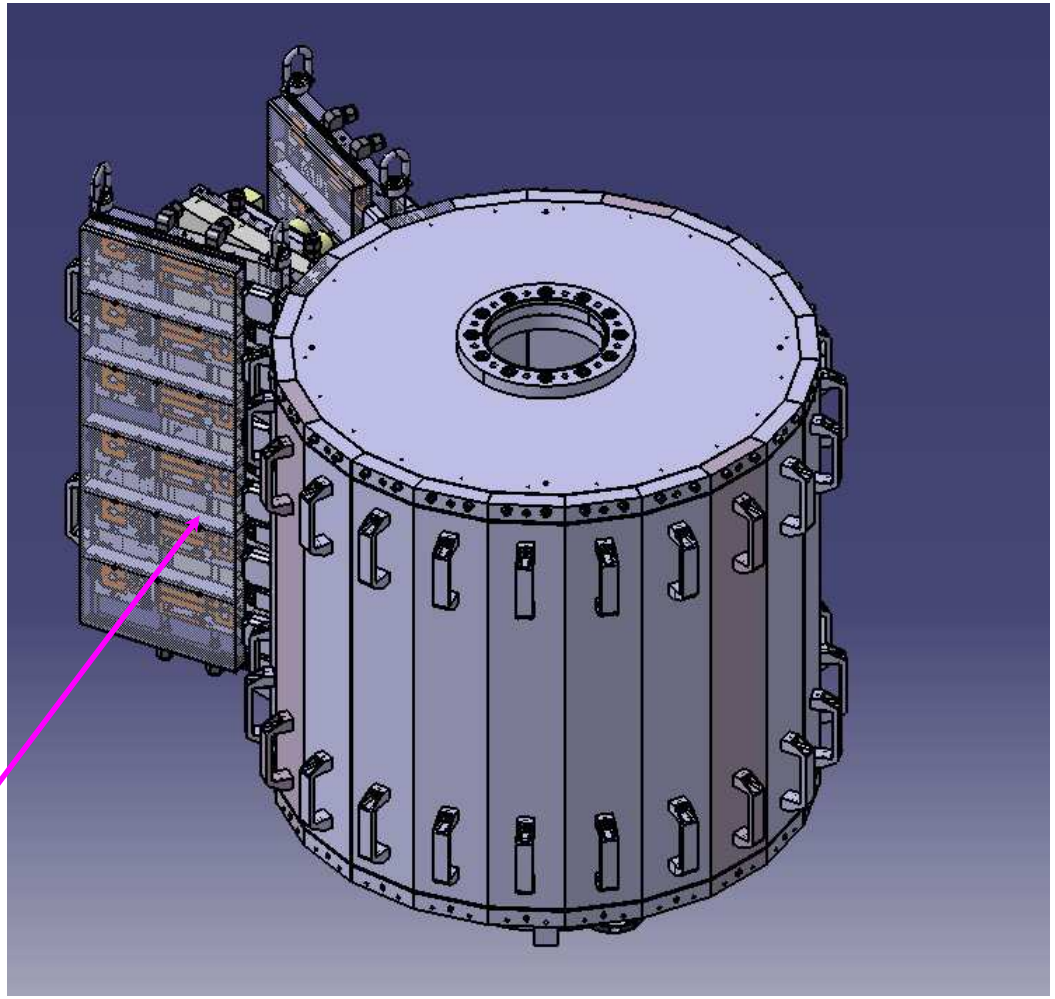
RF modules, individually shielded

AC/DC converter

The wings constitute the cylindrical cavity wall

Cavity combiner: modules implementation

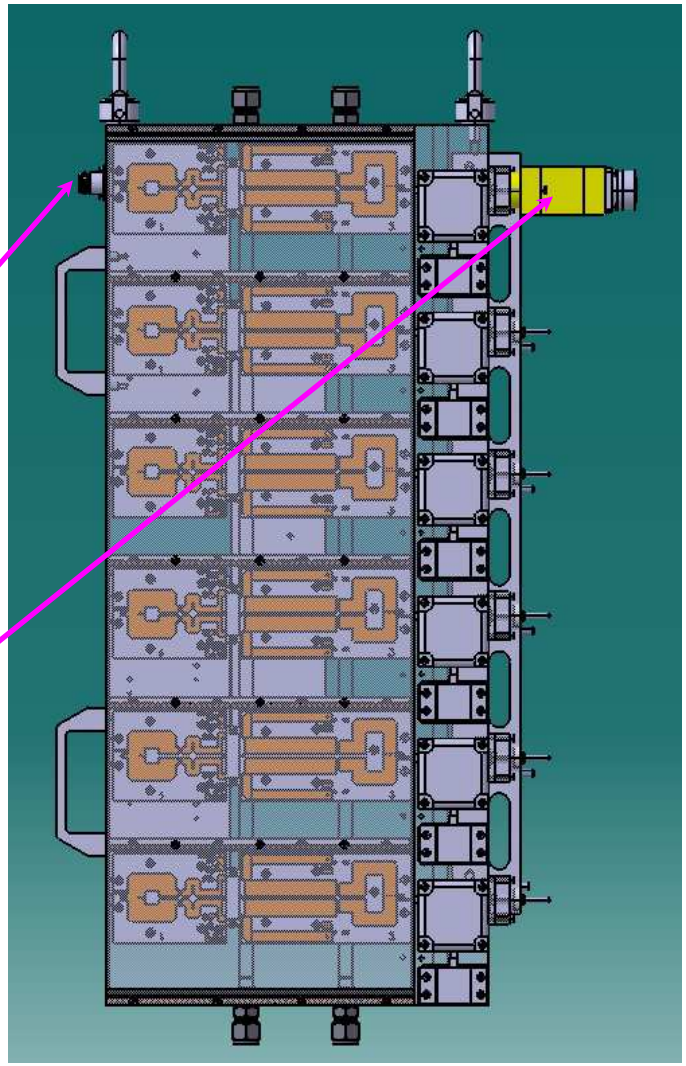
For the 10kW first step, the cavity is fitted with 3 adjacent (or not) “wings”. Each of them is equipped with 6 transistor amplifiers. They are all water cooled. The water feeding circuit has not been designed yet. It cannot use the ESRF deionized water circuit, because aluminum is forbidden on this loop.



RF modules globally shielded

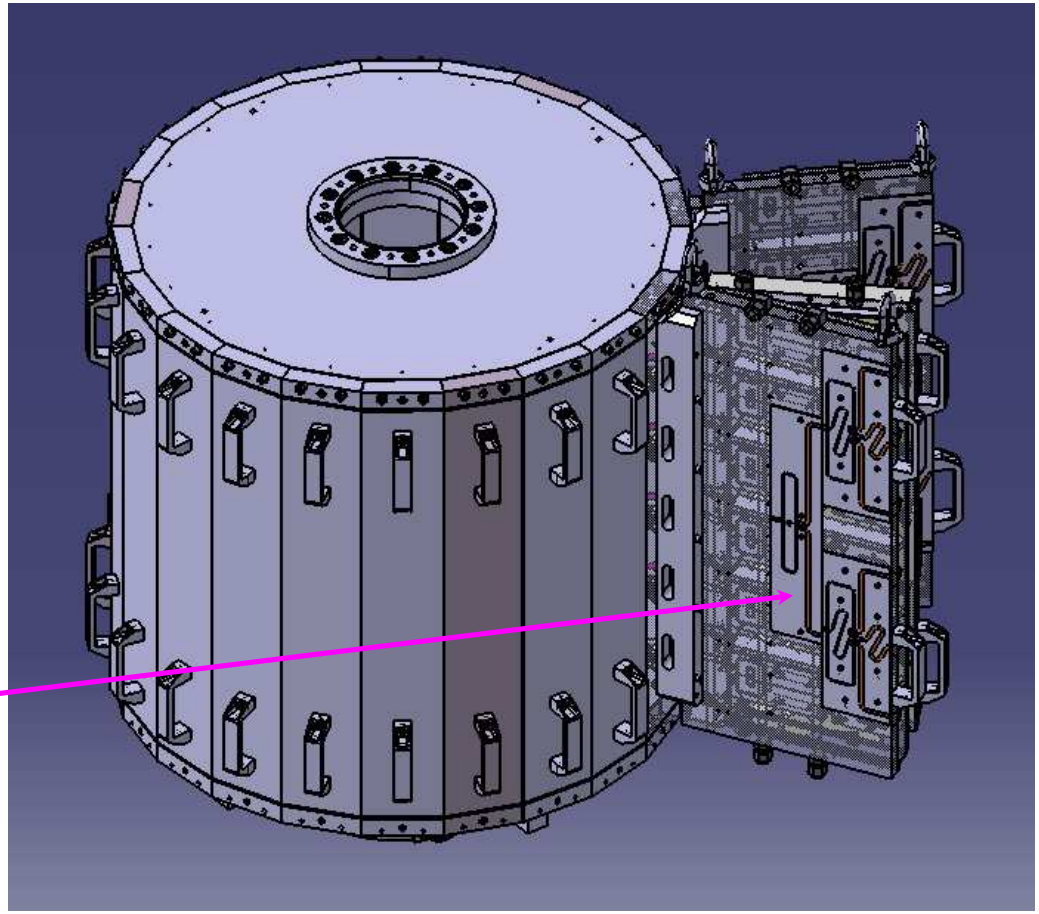
Cavity combiner: test fixture

For test purpose only, a 7/16 output connector can be fitted on the circulator output. A N connector is fitted at the input.



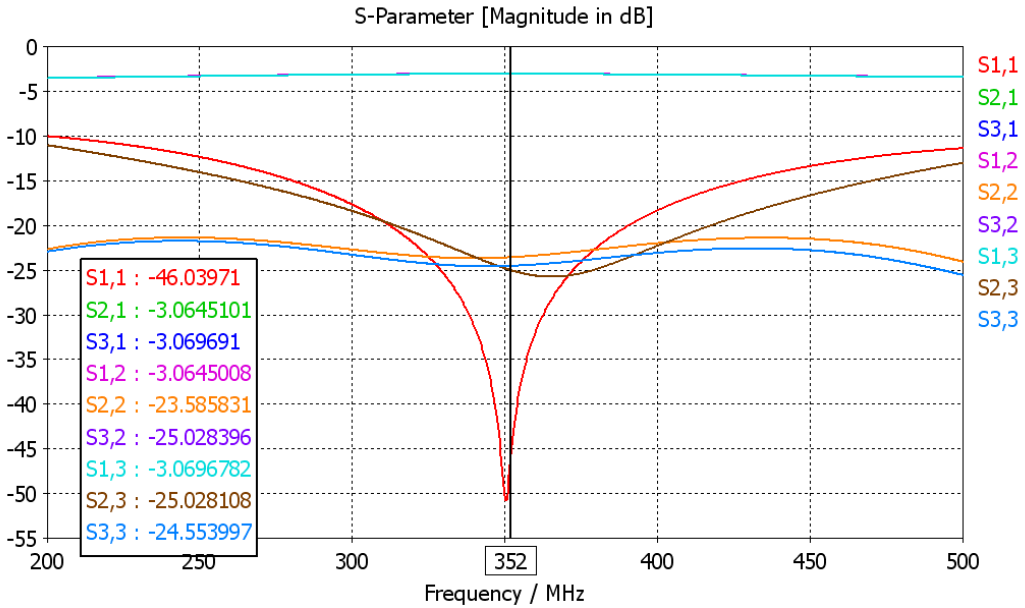
Cavity combiner: RF distribution

RF distribution is made with printed Wilkinson dividers to avoid connectors and cables. The 2 ways splitter is a delta Wilkinson, and the 3 ways is star connected.

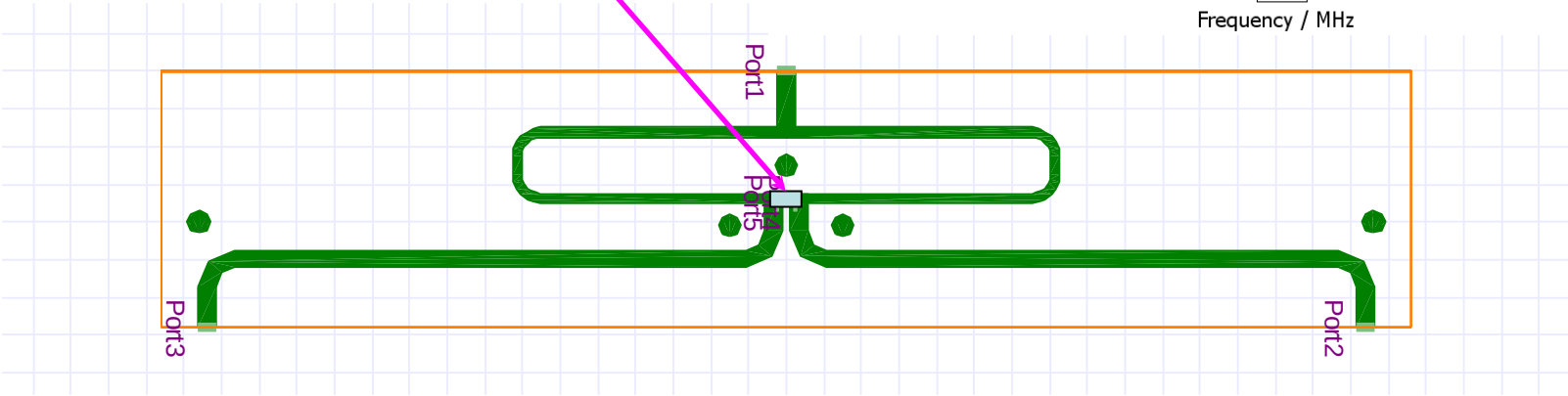


Cavity combiner: 2 ways Wilkinson divider

It uses 1.6m thick RT5870 (low ε) to avoid too thin lines and losses. The narrow shape helps minimizing the area, and hence the cost.

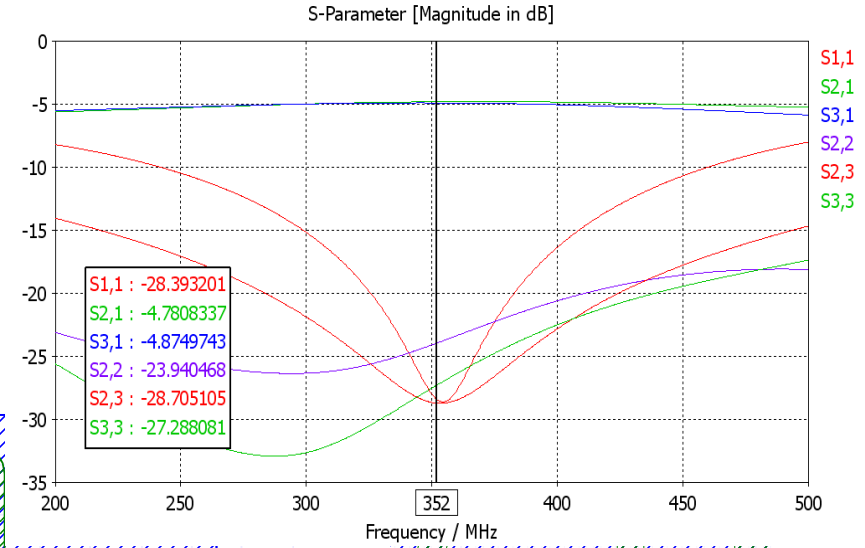


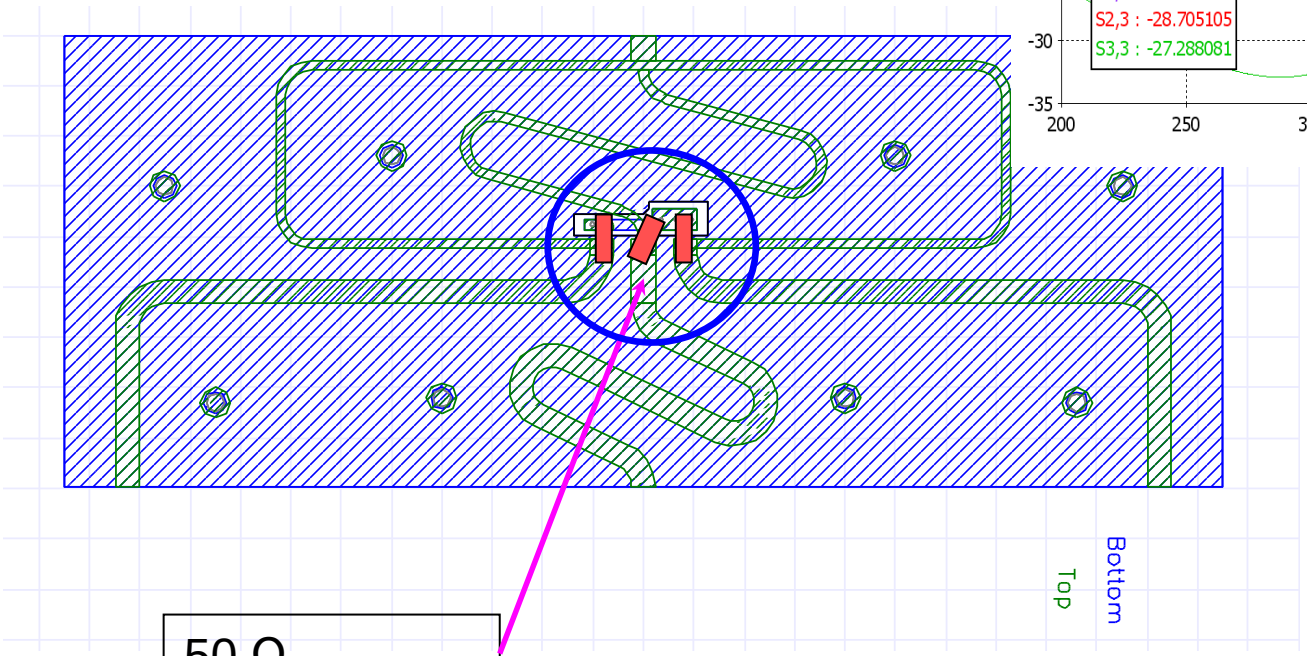
100 Ω resistor

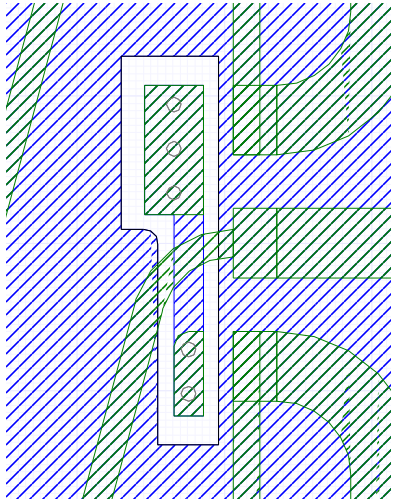


Cavity combiner: 3 ways Wilkinson star divider

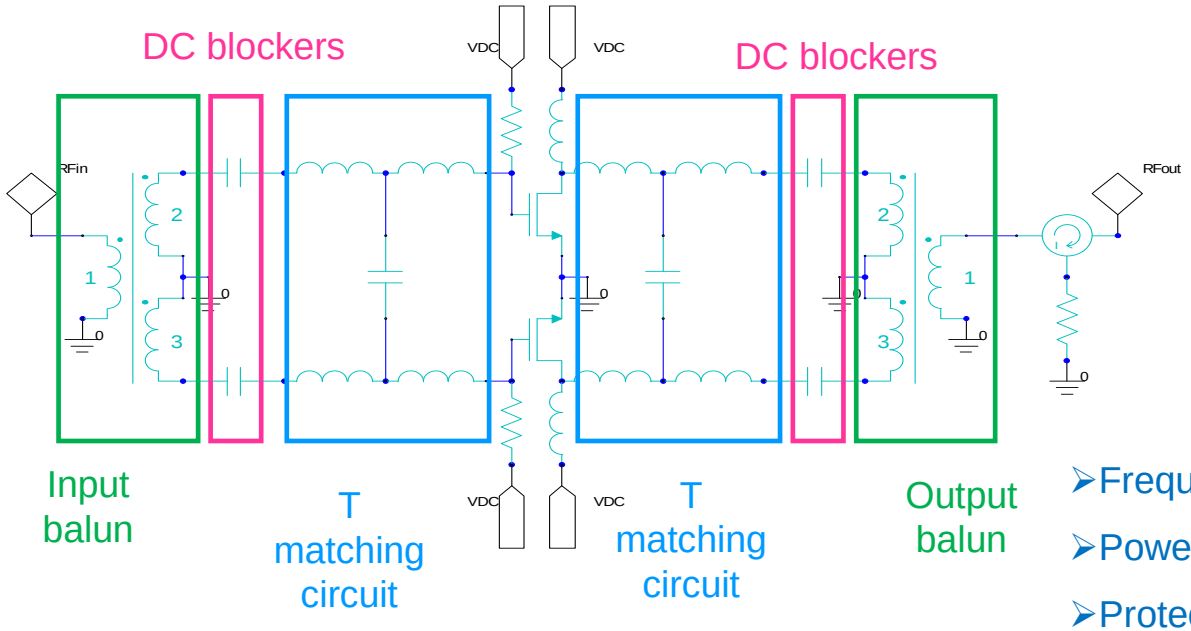
Same RT5880 (low ε) substrate. The strange shape helps minimizing the area, and hence the cost.







The RF module: Scheme



Targets :

- Frequency: 352.2 MHz
- Power: 800 W C.W. at -1dB compression
- Protected against V.S.W.R
- Bandwidth: >2MHz at 0.2 dB
- Drain efficiency: 70% at full power
- Low quiescent current
- Cost effective

The RF module: design options

Avoidance of components needing manual intervention

- No variable capacitors
- Suspended printed planar baluns
- No trimmer except for gate bias
- No RF chokes

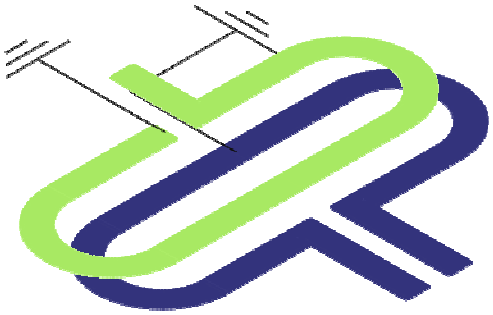
Transistor choice: LDMOS 50V

- NXP BLF578
- FREESCALE MRF6VP41KH
- Ruggedized version of the formers

Planar printed baluns

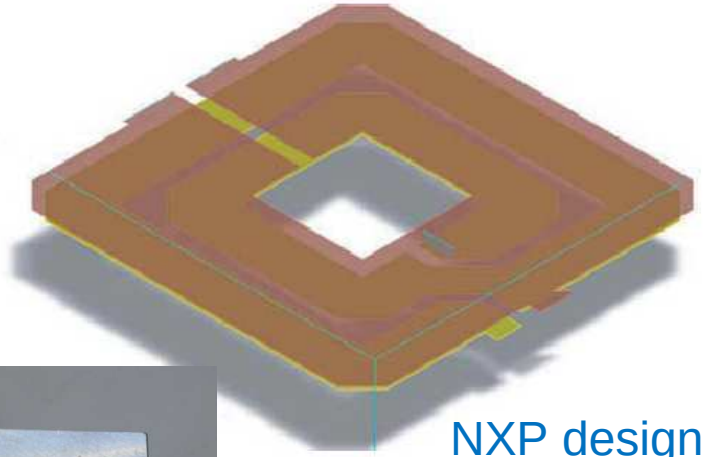
invented by Mr J.Bouny for MOTOROLA

unbalanced

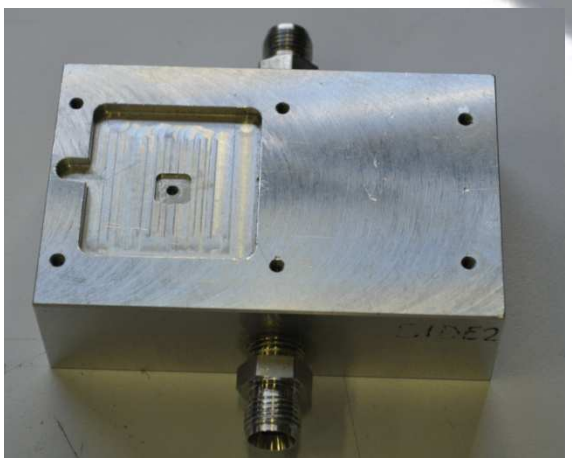


balanced

Balanced on top
Unbalanced on bottom



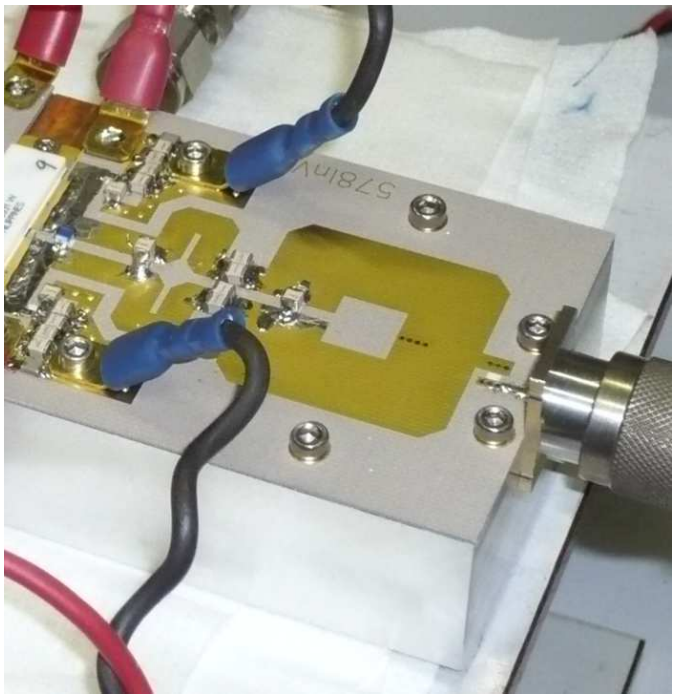
NXP design



The cooling plate has to be milled and the balun is difficult to cool

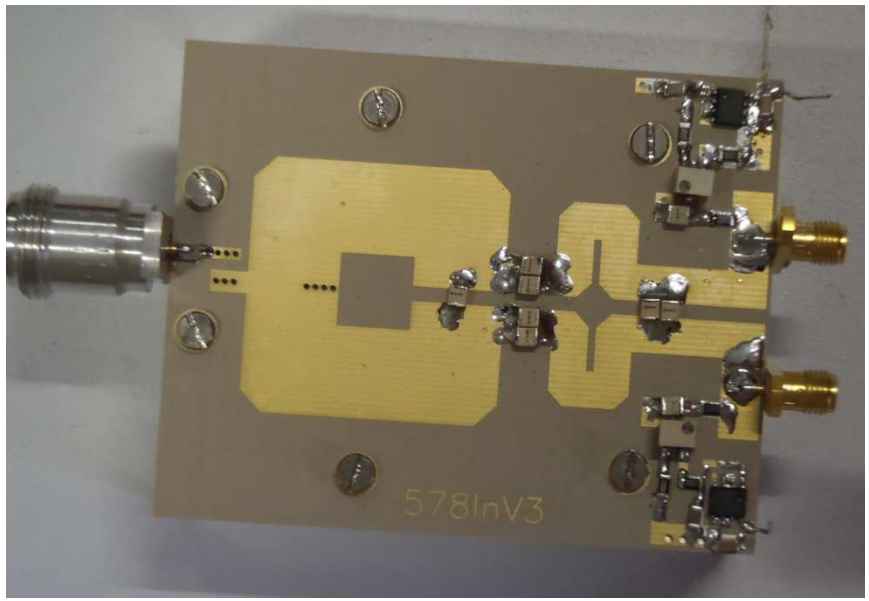
The RF module: input

V1

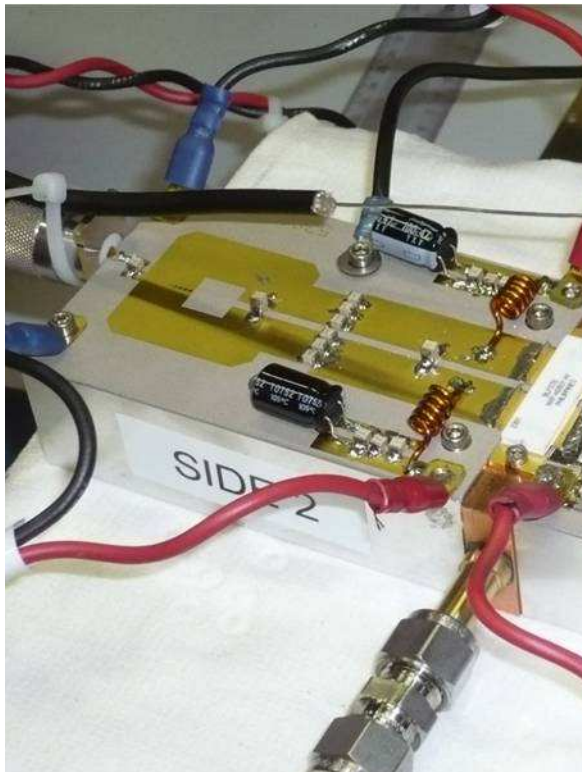


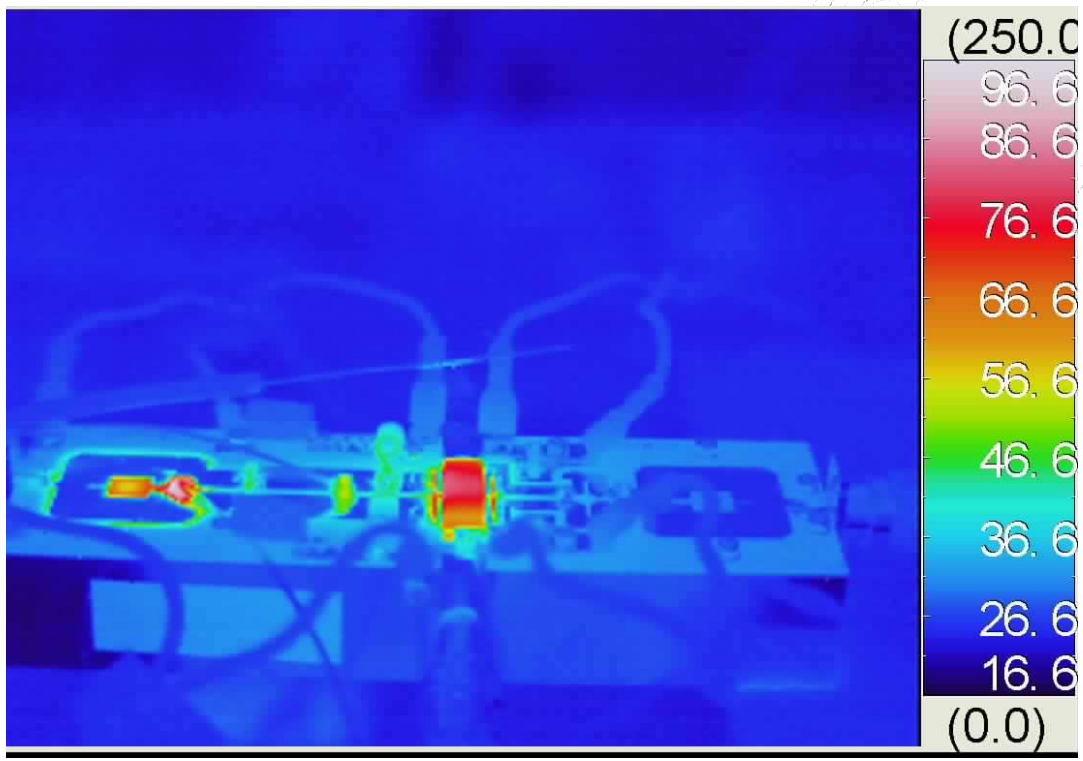
The input circuit printed circuit was OK from the start. The 2nd version has two bias voltage sources made from the drain voltage.

V3



The RF module: output



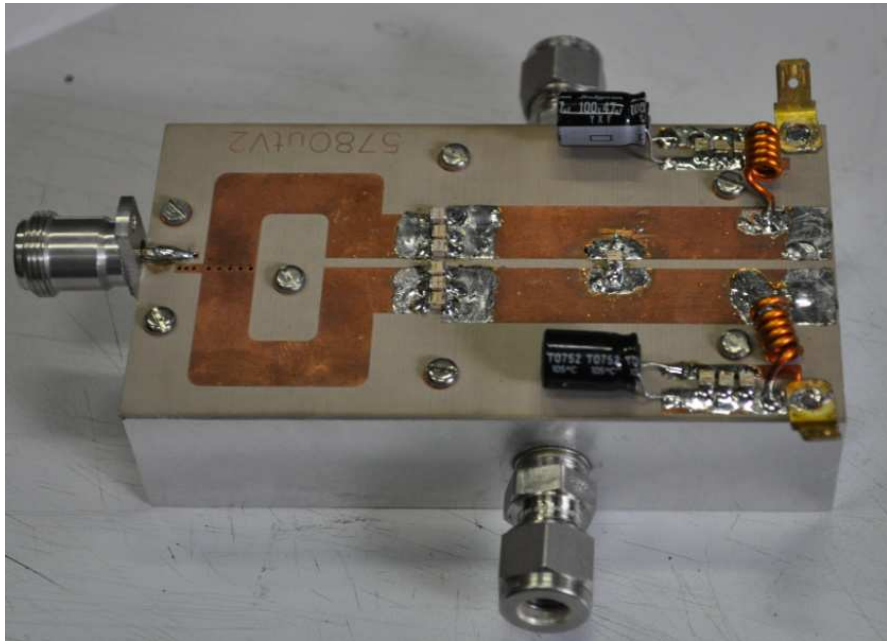


V1

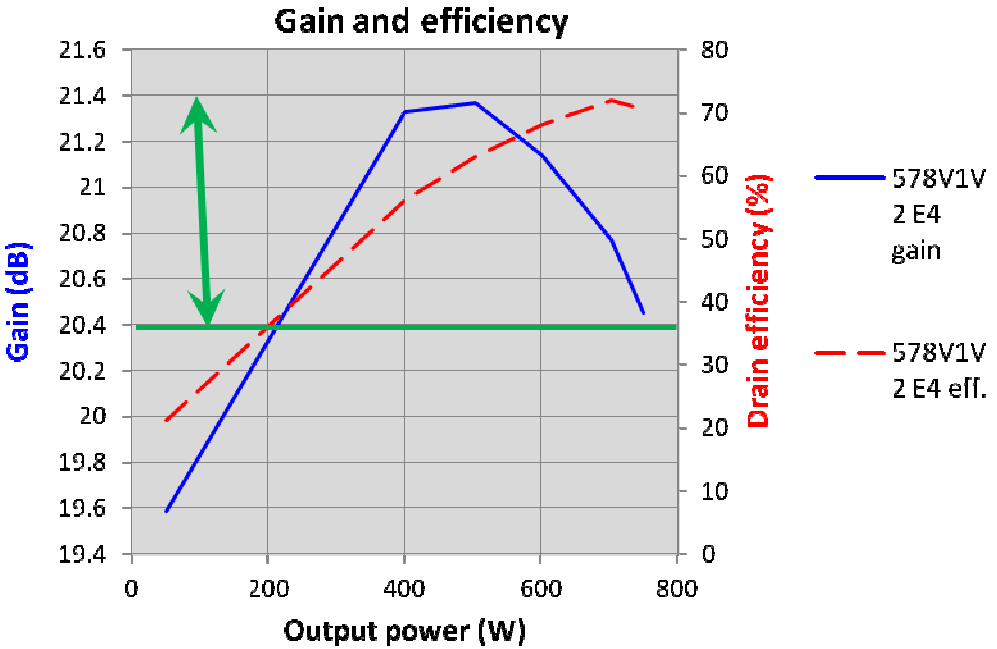
Substrate λ=0.24W/m*K

Overheating of the output balun and its matching capacitors.

The RF module output circuit: 578OutV21

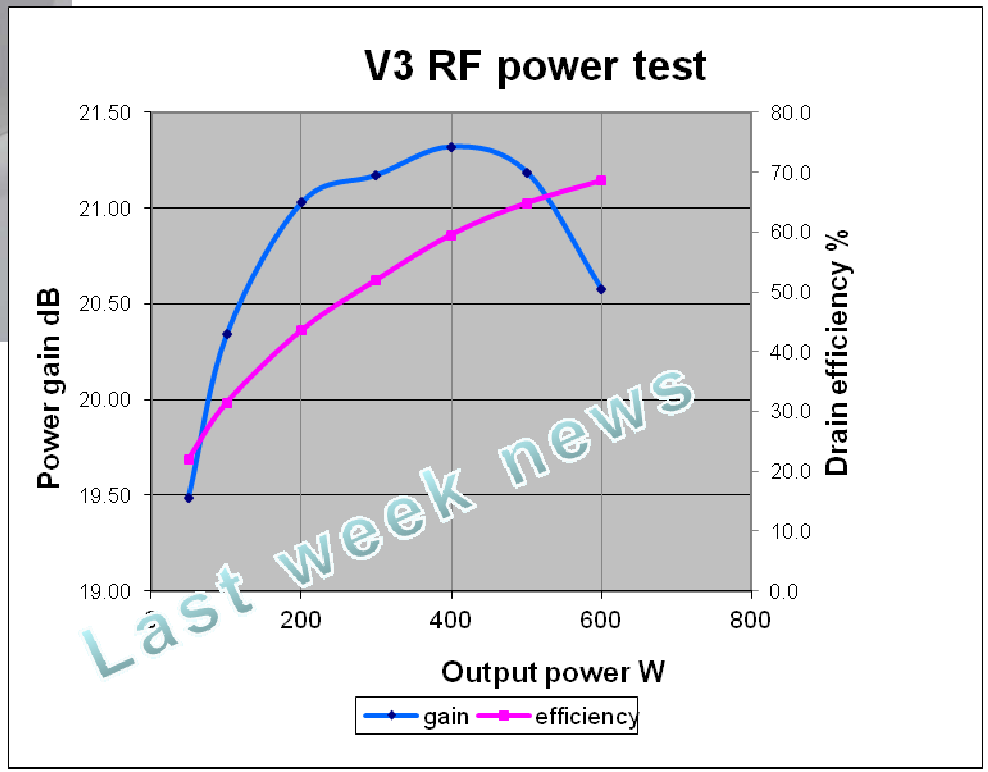


V21
High conductivity substrate
No capacitor on the balun



The RF module output circuit: 578V3V3

V3
RF drain chokes have been replaced with “quarter wave” transmission lines. Very few components are left, all of them CMS and prone to automated manufacturing in Europe.



The RF module: issues

- The results shown were obtained with the NXP transistor. It has to be repeated with the FREESCALE MOSFET.

- The power limitation comes from the transistor ESD protection diode, which conducts as soon as the input power reaches 6.4 W. This is probably the reason for the early saturation of the V3 version. The XR ruggedized version should not exhibit this drawback.

- The reproducibility has not been checked yet.

- The output matching capacitor is hot. Long runs have to be performed to make sure these temperatures are acceptable.

578V3V3 : prices

Bill of material:

For 20 modules, transistor and circulator included, 487€/module

For 150 modules, transistor and circulator included, 382€/module

Many thanks!

•To my colleagues of both the RF group and the design office, for their support.

•To Francis PEREZ (ALBA) who first dared to test the cavity combiner concept to combine 2 IOTs.